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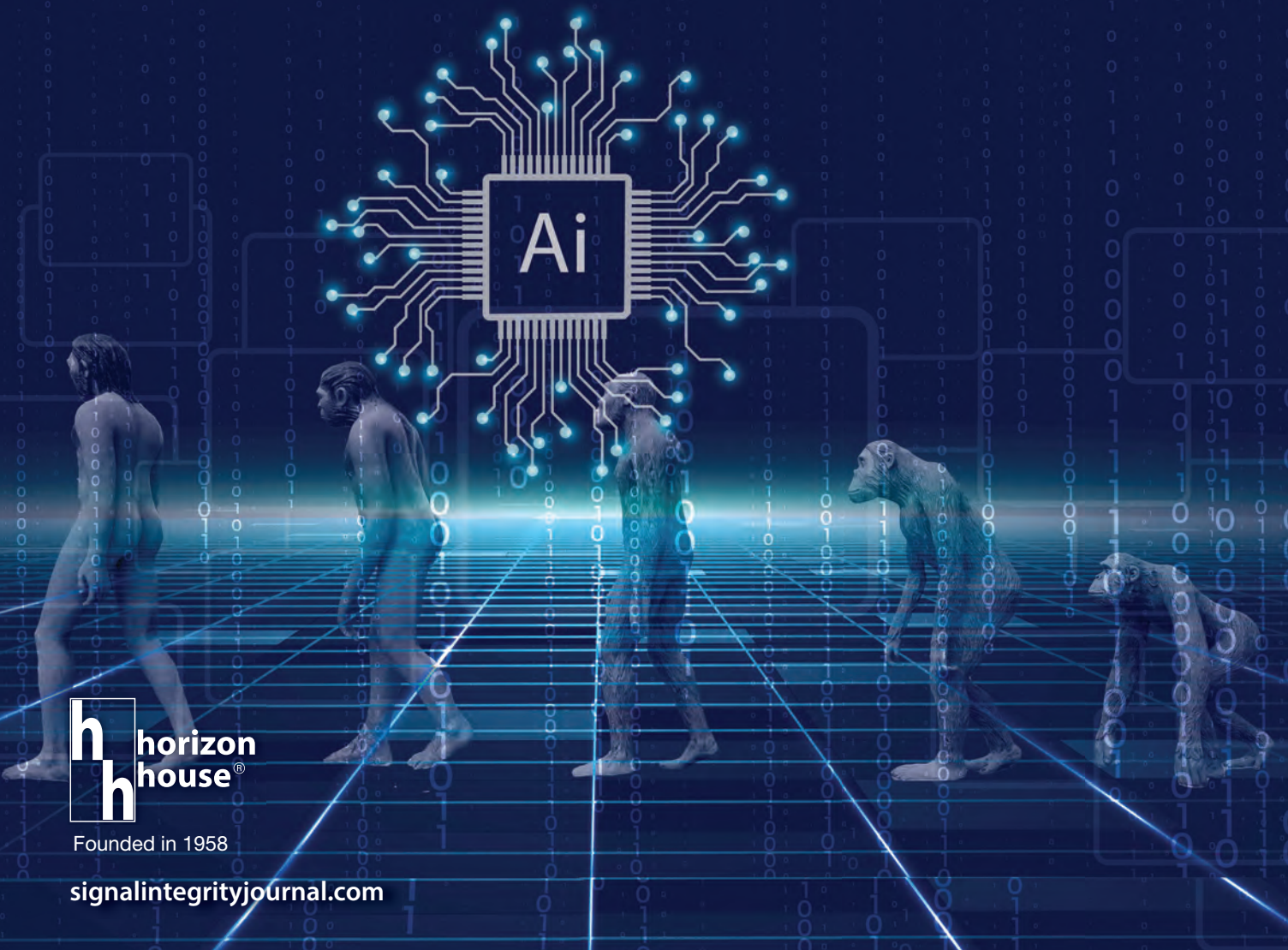
Cover Feature: p. 8

The Road from 1 Gbps-NRZ to 224 Gbps-PAM4

DesignCon Preview: p. 56



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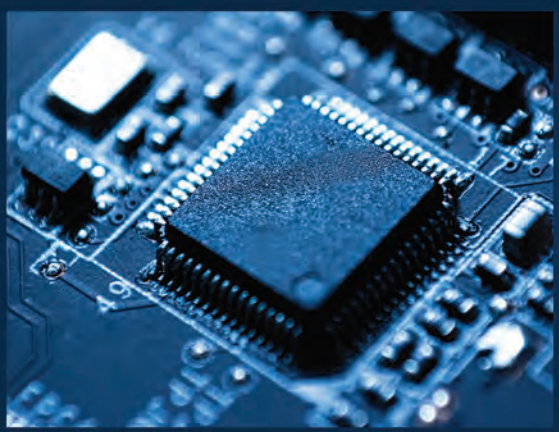

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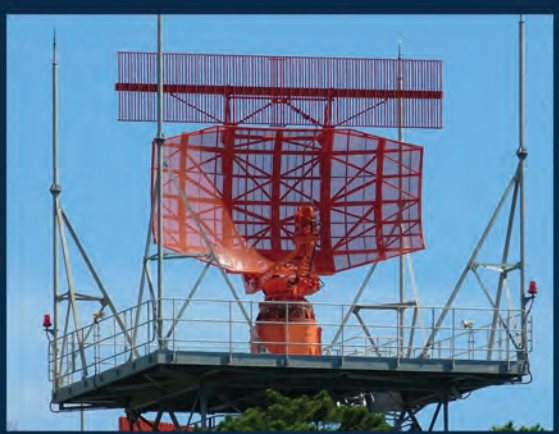

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Generative AI is in Your Future

Eric Bogatin, Technical Editor
Signal Integrity Journal

In just two generations, we have lived through six different technological revolutions that have transformed our economy, our careers, and our quality of life, for better or for worse. Generative AI is the latest.

The electronics revolution began in 1947 with the demonstration of the first transistor. Electronics are now part of every product, in every application across every aspect of our daily lives. Just recently, Nvidia announced the volume production of a single processor with 28 billion transistors, with devices planned in the next generation approaching 90 billion transistors.

The first personal cell phone was demonstrated in 1973. Today, there are over 6.8 billion cell phones in use. We have come to take for granted having access to instant communication with anyone around the world and 24/7 access to every movie, document, and piece of information ever created.

Information processing is an emergent application of the electronics revolution that enables embedded intelligence everywhere, from the microcontrollers in every appliance to the fastest supercomputer, the Frontier computer system at the Oak Ridge National Laboratory, which has more than 8 million cores and is capable of more than one exaflops.

The combination of electronics, intelligence, and mechanical action is the driving force behind the revolution in mechatronics. This spans the range from tiny micro-electromechanical systems, such as MEMs-based robots that travel through bloodstreams, to the robots that assemble cars.

It may be too late to have as profound an impact as is hoped, but the revolution in electrification is accelerating. All devices that are mobile, from personal devices to cars and planes, are migrating to battery power. Those devices, which must be tethered to a local power source, are connecting to the grid, which is evolving to enable multiple power generation sources. We are in the early phases of the electrification revolution. Stay tuned to see the impact it will have on all of our lives.

The sixth technology revolution that is accelerating in maturity is artificial intelligence (AI). The origins of AI had their start with pioneers such as Norbert Wiener's cybernetics in the 1950s, and Marvin Minski's neural network, SNARF, in the 1960s. Today, neural network-based machine learning algorithms have permeated many applications, such as ordering at fast food restaurants and autonomous cars.

The latest twist in the AI revolution is generative AI. The public was recently introduced to generative AI with the release of Chat Generative Pre-Trained Transformer (ChatGPT). While some have referred to this type of program as a glorified word completion application, it is becoming apparent that it is much more.

To learn more about generative AI, I took the natural next step and asked ChatGPT to tell me more about generative AI and its future. This is its (or should I say his, or her?) response:

"Generative AI is a subset of artificial intelligence that uses learned patterns to produce new data, such as text, images, or music, closely resembling existing examples. The future of generative AI holds promise in diverse fields. Enhanced creativity, personalization, and problem-solving capabilities will transform content creation, art, and research."

The combination of all these technological revolutions and AI will affect our industry in two ways: firstly, how the electronics revolution will evolve to enable evermore powerful AI-powered systems, and secondly, how the application of AI systems will accelerate the design of evermore advanced electronic systems. It is sort of the ultimate form of introspection and self-replication: AI systems will help design the next AI systems.

I recently had the privilege of moderating a panel on "Designing 224G PAM-4 Systems for Generative AI Architectures," with four industry experts: Karl Bois from Nvidia, Lennin Patra from Marvell, Gus Panella from Molex, and Chris Kapuscinski from Molex. A recording can be viewed here: www.signalintegrityjournal.com/Generative-AI.

Three themes emerged from this panel that may have an impact on how future 224G systems are implemented.

Generative AI systems are parallel processing driven. Problems are parsed into many smaller pieces, each processed in parallel. Coherency between each branch is important. There is less overhead available for resending packets due to transmission errors, requiring a lower bit error rate than more resilient systems.

The design challenges span not just signal integrity, but mechanical integrity, power, thermal management, software, and manufacturability. This may create new working relationships between all the engineers across various companies who must come together to build a successful product.

Using the traditional approach of interface specs between modules and interoperability may cause the design margins to shrink below zero. Every AI system may end up being a custom, proprietary system with its own set of tradeoffs and system level optimization that drives design decisions rather than attempting any sort of interoperability.

The six revolutions we are all engulfed in have had a profound impact on our daily life. Generative AI will affect the daily lives of engineers, both inside and outside of our work.

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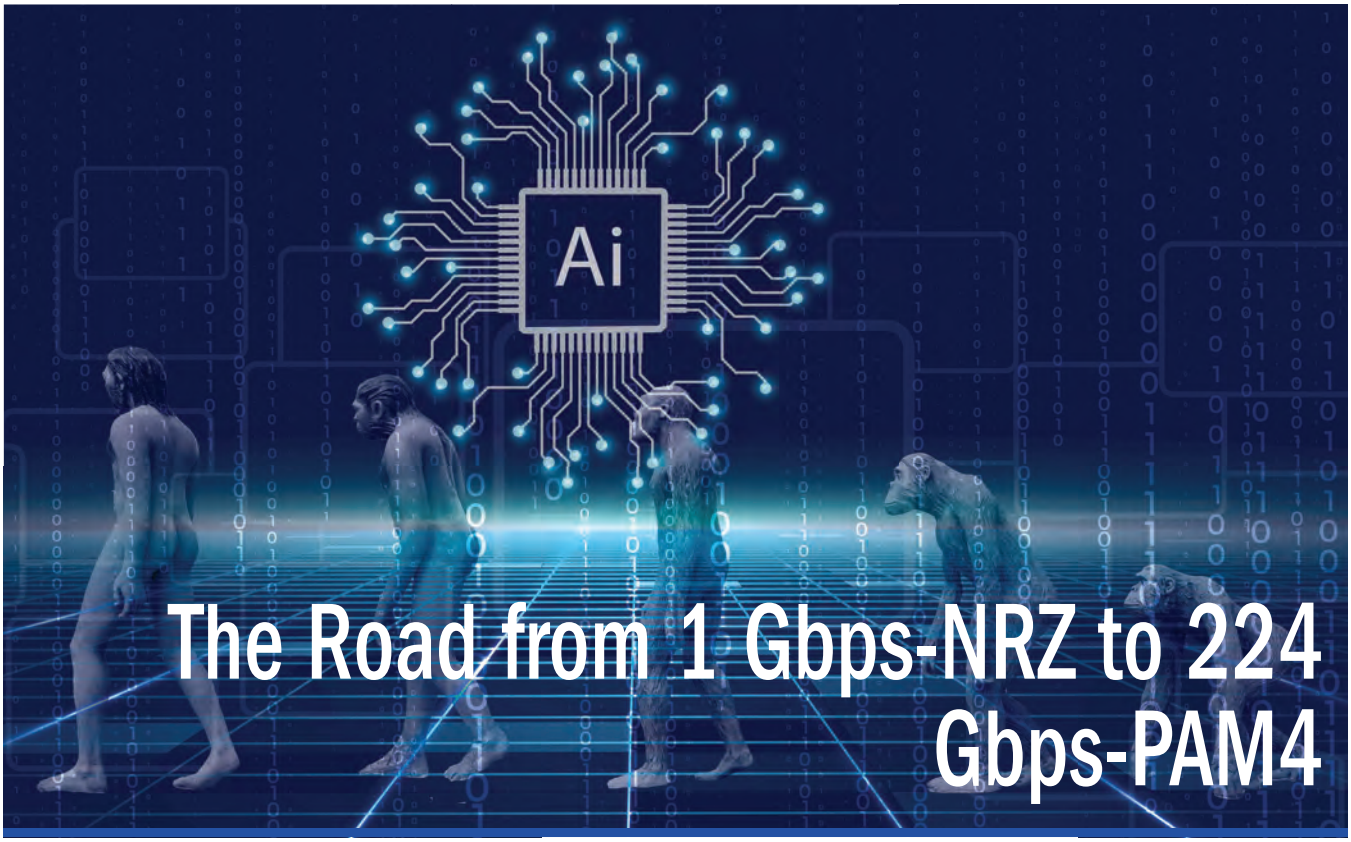

The Road from 1 Gbps-NRZ to 224 Gbps-PAM4

Augusto (Gus) Panella
Molex, Lisle, Il.

Semiconductor signal conditioning and signal recovery innovations have extended data rates by managing allowable signal-to-noise ratio (SNR) at progressively higher Nyquist frequencies. We have experienced how each successive signaling technology increases the electro-mechanical design resolution needed to address the channel physics while respecting the SNR of the chips. These movements throughout the years have provided a baseline of traditional design goals that lead us to better understand today's 224 Gbps-PAM4 (Pulse Amplitude Modulation) physical layer requirements.

Historical Evolution

As we move through the speed grades, the physical layer design of printed circuit boards (PCBs), cables assemblies, and connectors evolves. The latest data throughput and latency-driven signaling updates challenge previously acceptable design trade-offs.

The requirements for high-speed data transmission continue to increase to meet market demands, including cloud computing, artificial intelligence, 5G, and the Internet of Things. Although there are overlaps in the details, a brief overview of how we got to where we are today will help illustrate the technological progression from 1 Gbps transmission line data rates to the 224 Gbps rates of today.

Approximately 30 years ago, the discussion centered around return to zero (RZ) versus non-return to zero (NRZ). Most signaling inside the data center (within or between boxes) was single-ended until twisted-pair Ethernet came along.

Let's not forget about those adventurous engineers at Cray, who pushed the envelope to support NASA workloads running across multiple compute nodes at 80 MHz data rates using differential pairs. In comparison, the first IBM PCs around the same time were clocked under 4.77 MHz.

This is when processor clocks were divided instead of multiplied. PCBs moved from wiring boards to multilayer FR4 and were literally "taped-out" by hand using actual tape; multiwire cables were used for printers and coax for networks; RJ-45 was used for telephones; and integrated circuits replaced individual components on printed wiring boards. In the lab, it was still possible to prototype circuits using protoboards and measure signals with an oscilloscope. For simulation, lumped values (L, R, C, k) were sufficient to model most discontinuities.

Roughly 20 years ago, NRZ signaling started to dominate the mental model. Moving from 1 Gbps-NRZ to 3 Gbps-NRZ and then 6 Gbps-NRZ, each data rate step increased mechanical/electrical design attention on geometrical changes, but generally still treated the connector or PCB as a lumped loss component.

The introduction of NRZ design requirements effectively doubled the channel bandwidth while being more susceptible to noise. To reduce data errors, SNR was improved by increasing power and adding equalization techniques.

Electronic design automation (EDA) for PCBs started to arrive along with Gerber files. Connector technology for data included the edge card and 9-pin d-sub. Scope probe loading neared its limit, vector network analyzers (VNAs) became commonplace, and Fast Fourier

Transform (FFT) analysis became prevalent. For simulation, lumped values (L, R, C, k) were sometimes in place, while behavioral SPICE models were incorporated in transmission line simulations to simulate discontinuities.

About 15 years ago, the transition started moving from 10 Gbps-NRZ to 16 Gbps-NRZ and then 25 Gbps-NRZ. Backplane cables emerged as the norm, with many companies creating backplane demonstration boards to mimic applications with 1 m trace lengths.

As a result, lumped component models for connectors or transmission line discontinuities were no longer sufficient. Although common in the RF industry, everyday bond wires, PCB vias, and connector segments were represented with their own S-parameter components. Crosstalk evolved as an increasingly critical consideration in the design space.

Signal integrity labs had 50/100 Ω data generators with high-bandwidth sampling oscilloscopes for time domain analysis. Next to every time domain test system was a VNA. Sometimes high frequency probe stations were used, but most of the test fixturing was based on SMA launches. Around this time, a specialized group of signal integrity practitioners emerged from the electrical engineering ranks.

Just around 10 years ago, the march from 28 Gbps-NRZ to 56 Gbps-PAM4 began affecting transmission line design while representing an important signaling change in modulation from NRZ to PAM4. With the goal to further increase data rates, the industry adopted PAM from the optical industry. "PAM4" is ubiquitous in the optical domain, which made it easier to adopt into long-reach copper interconnects compared to other modulation schemes.

In copper, PAM4 uses four voltage levels to represent two-bits of data per symbol. By encoding two or more bits per symbol, PAM increases the data rate without increasing the required channel bandwidth. The consequences to signaling and transmission line design include greater sensitivity to noise and insertion loss deviation.

This generally transitioned the industry from 28 Gbps-NRZ to 56 Gbps-PAM4, or in the case of PCIe, from 32 Gbps-NRZ to 64 Gbps-PAM4. The application space was either networking or computing. In both cases, the channel design respected the same unit interval (UI) and Nyquist frequency. The downside was resulting multiple signaling levels required a better channel SNR, forcing specific attention to unintentionally couple signals (crosstalk) and insertion loss.

This step placed greater emphasis on crosstalk, especially near-end and on transitions between components: connectors-to-PCBs, connectors-to-cables PCBs, and connectors-to-connectors. Test equipment in the lab was primarily VNAs. Reducing stubs in PCBs (backdrilling) and connectors was the new mission.

The correlation between measured S-parameters and predictive analysis for high frequency simulators became critical to ensuring that time domain simulations could properly estimate bit error rate (BER). With Ethernet for cloud computing and IoT, the line data rate went from 56 Gbps-PAM4 to 112 Gbps-PAM4, doubling the Nyquist frequency to approximately 28 GHz to support the 112G-PAM4.

Design attention focused on impedance transitions along shorter connector paths and electrical stubs ~1 mm and longer. At the same time, channels went from 16 lanes to 32 lanes, doubling the effective throughputs in the same amount of front panel space.

Density increases were directionally opposite to design methods that separated lines to reduce noise. Instead, transmitter and receiver pair groupings are commonly used to reduce near-end coupling impact. Selective channel grouping in PCB uses different layers for transmit and receive to reduce noise. Connector designs purposely put larger physical gaps between transmit and receive pairs.

Electrical labs and production lines use 67 GHz VNAs. Engineers typically do time domain analysis with production silicon. As a result, signal integrity engineering has emerged as its own discipline.

Emerging Technology

The transition from 112 Gbps-PAM4 to 224 Gpbs-PAM4 doubles the Nyquist frequency. Previously, speed transitions took three to five years. Now, we see 224 Gbps-PAM designs happening before 112 Gbps-PAM4 has even had the chance to become a volume leader.

Signal integrity engineers now are worried about stubs, transmission line discontinuities, and apertures of ~0.7 mm. This means we are now sub-mm in our design space. To put this in perspective, the entire channel can be over 1 m in length, with each discontinuity interdependent on physical transitions both before and after the immediate area of concern.

Wavelengths are now small enough that typical apertures (resonance cavities) are as important as the signal path. Apertures, whether in the signal, return path, or between components, have become a critical part of transmission line design.

224 Gbps-PAM4 Design Challenges

For a clearer understanding of how 224G-PAM4 targets impact design, let's consider basic signal integrity challenges of correlation, transmission-line imbalance, and within pair skew.

Model-to-Measurement Correlations

Meeting time-to-design (a step earlier than time-to-market) requires advanced predictive analytical techniques and methods. It is not always possible to build and tune the physical channel times before engineering silicon arrives, which means the models need to be as accurate as possible. In addition, any deviations between modeled and predicted correlations must be understood to meet time-to-design goals.

In the frequency domain, removing errors from test boards is critical. The improvement cycle includes test equipment, test fixturing, calibration (fixture removal), and test boards. With these systems often costing close to $1M, it is also worth considering what is absolutely required in the production environment.

It's increasingly critical to have design correlation between measurements and models. Any errors that are in the frequency domain can show up in the time domain. For "measurement to model" correlations, the

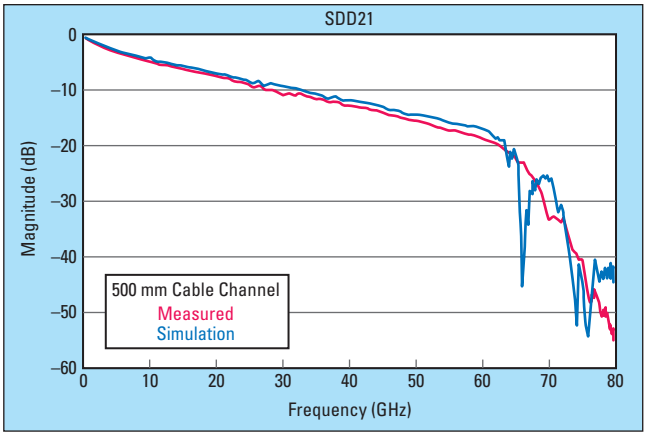

Fig. 1 Insertion loss plot of a two-connector channel example consisting of a connector and 500 mm cable assembly.

following scenarios should be considered:

- If measurement is worse than modeled, how do you respond?
- If measurement is better than modeled, what do you believe?
- What is a good correlation? Within 1 dB?
  - If yes, for which frequency parameters?
  - How do each frequency domain parameters impact eye closure?
  - How do each frequency domain parameters impact BER?

Consider a two-connector channel example consisting of a connector, 500 mm cable assembly, and another connector. In ***Figure 1***, the measurement shows greater overall loss, but does not have the 60 GHz+ resonance spikes shown in the simulation. Considering a Nyquist of 56 GHz, which is more pleasing, depends on the design budget and method.

Unfortunately, when in predictive mode, we do not know the actual results. If the insertion loss is within budget, should we be pleased with this alignment? If only considering the predictive results, time would be spent removing the resonance spike when it may have been more effective to focus on lower frequency losses.

Early measurements improve focus. In this example, knowing there is a difference between the simulation resonance spike and the measurement's smooth roll-off helps us understand the actual channel, and therefore improve the time-to-design. The difference in the insertion loss will aid in directing a better understanding of the physics associated with broadband response.

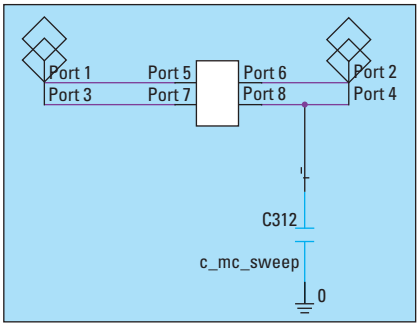

Fig. 2 Model of a two-connector channel example consisting of a connector and 500 mm cable assembly with an intentionally added perturbation.

Transmission Line Imbalance

Let's consider the same 500 mm channel from the example above. But this time, let's intentionally add a perturbation (see ***Figure 2***). In the real world, this could represent a mismatched solder volume between the P and N wires.

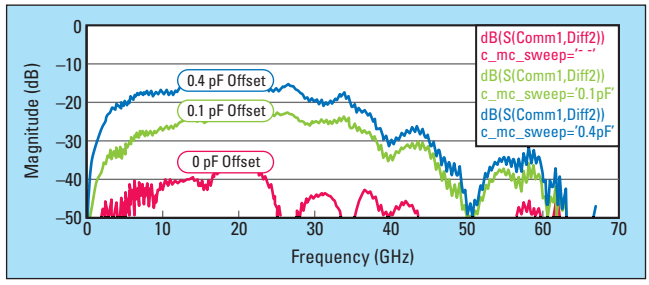

Fig. 3 Insertion loss plot two-connector channel example with intentionally added perturbation. From bottom to top: Ideal balanced channel to others with increased capacitive offsets.

The two-connector channel is contained in the center S-parameter block. A quick run of the simulator shows an impact in mode conversion. The mode conversion change is interesting, but may not reveal the actual impact on system performance (see ***Figure 3***).

Taking the next step, let's look at the impact on the eye diagrams generated from pseudorandom binary sequence bitstreams (PRBS). With no signaling compensation on either the transmit or receive sides, this shows us something a bit more interesting (see ***Figure 4***). Even at 0.1 pF of imbalance, we have reduced the eye opening, resulting in a lower channel margin.

Within Pair Skew

During the design process, there is much time and energy spent on eliminating skew from transmission lines. Skew is certainly important for reasons others in the industry have highlighted.

The channel in the example below is pad-to-pad as before, but in this instance, it has two cable assemblies interconnected for a total length of over 1 m. This is a three-connector channel example consisting of a connector, 200 mm cable assembly, connector, 500 mm cable assembly, and another connector.

For this study, there is a lossless delay artificially added on one of the lines that could be a PCB skew impairment as shown in ***Figure 5***. The three-connectors are contained in the center S-parameter block.

If we extend one of the lines of the differential pair by a small amount, again we notice an impact on mode conversion (see ***Figure 6***). As before, the mode conversion change is interesting, but may not reveal the actual impact on system performance. Did you also notice these mode conversions are not particularly different than the transmission line imbalance?

The eye diagrams in ***Figure 7*** shows that moving from the ideal channel to one with a different amount of skew impacts the eye diagram. From the data integrity perspective, even at 5 ps of delay, there is an appreciable reduction in eye opening, resulting in a lower channel margin.

In summary, time domain eye closure and frequency domain mode conversion can have similar responses caused by different aberrations. Be sure to look at minor design and process variations when evaluating how frequency domain lab results are represented in time domain.

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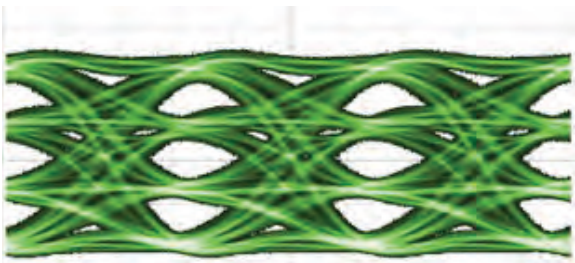

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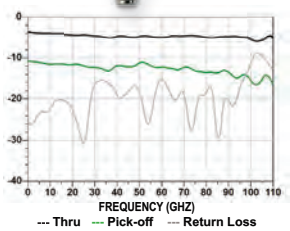

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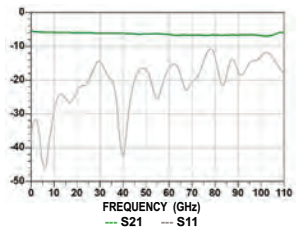

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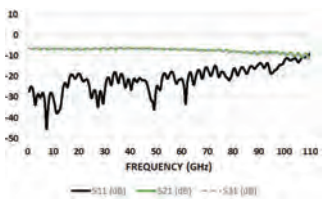

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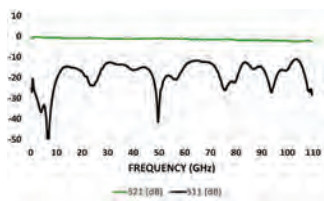

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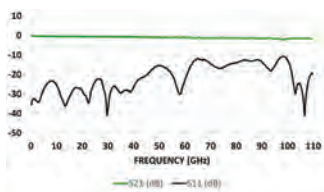

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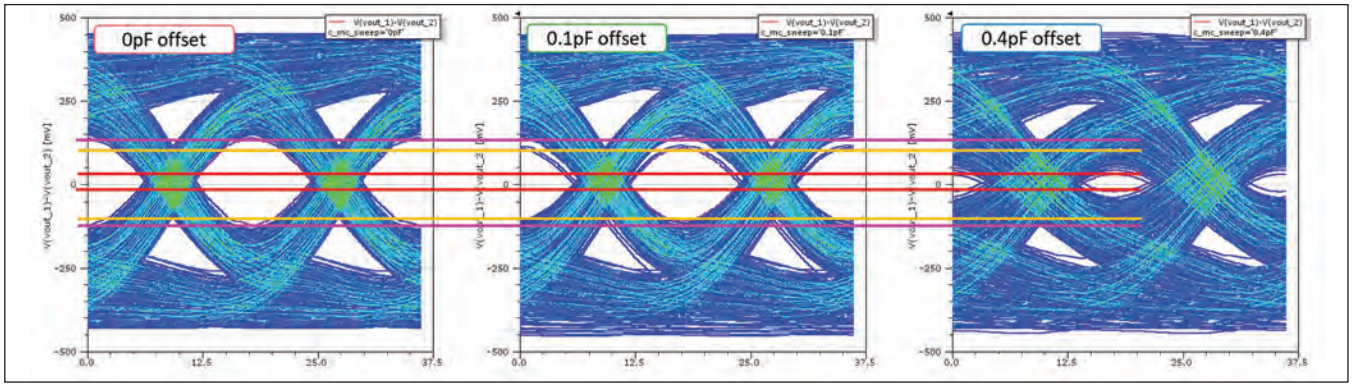

Fig. 4 Eye diagrams generated from pseudorandom binary sequence bitstreams for tow-connector channel example. From left to right: Ideal balanced channel to others with increased capacitive offsets.

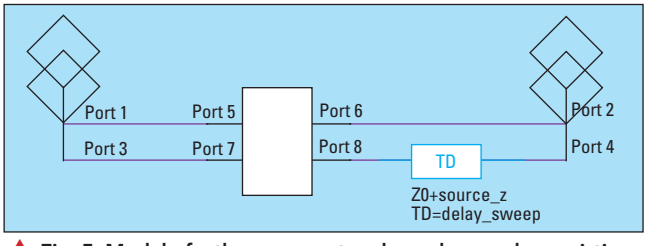

Fig. 5 Model of a three-connector channel example consisting of a connector, 200 mm cable assembly, connector, 500 mm cable assembly, and another connector with a lossless delay added.

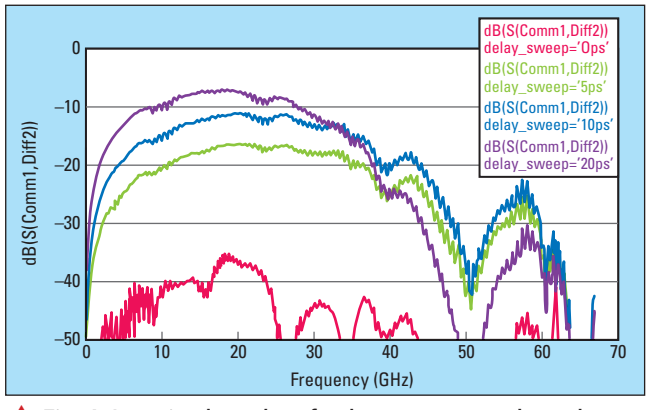

Fig. 6 Insertion loss plot of a three-connector channel example with a lossless delay added. From bottom to top: 0 to 20 ps of artificially introduced skew.

Design Considerations for 224 Gbps-PAM4

- A cross-functional design approach is best: System architects working in collaboration with cable/connector and semiconductor teams to support an application is the fastest way to a channel. Teams need to engage early in the channel development process to deliver extensible and scalable architectures. Important roles and areas of concern include hardware engineering, system architects, signal integrity, mechanical integrity, and thermal.
- Define performance targets first, specifications second: Start with targets giving contributors a chance to co-develop operational budgets that can later be broken down into components. Be transparent with margins. Specifications then come from operational prototype and correlated models.
- Confirm with correlation: Make sure there are model-to-measurement correlations for both S-parameters and time domain. Understand how frequency domain parameters relate to the time domain results.
- Applications need both signal integrity and mechanical integrity: Even as the signal requirements become more critical, the signal density requirements (differential pairs per square) continue to increase between generations. This means greater design effort is needed for mechanical parameters such as normal forces, mechanical robustness, and wipe. All of these intertwine with the application form factor (server chassis and cooling). Small deviations from intended design can reduce channel margin.

Conclusion

Application needs have driven data transfer speeds from 1 Gbps-NRZ to 224 Gbps-PAM4. Each step forward requires a better understanding of transmission line design, material physics, and system architecture options to scale to the highest density, mechanically robust physical layer. There is still engineering to do in 224 Gbps line rates; fortunately, today's tools and methods are better than ever and continually improving. Looking ahead, it will be interesting to see what the next 30 years will bring.

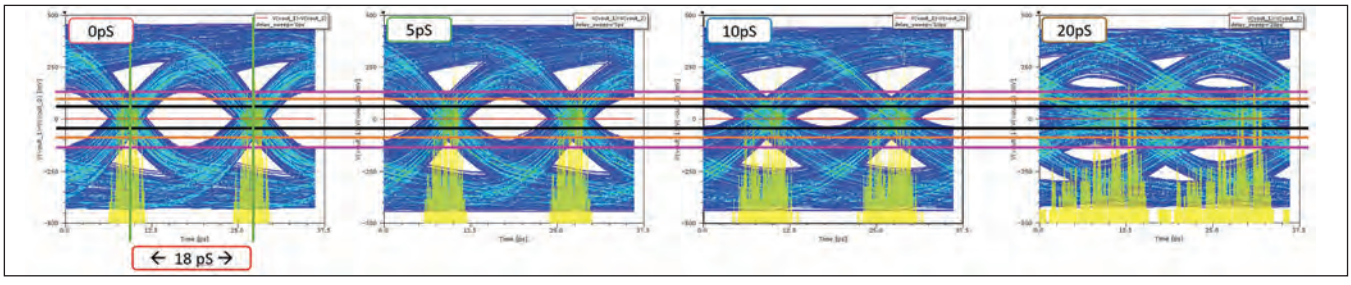

Fig. 7 Eye diagrams generated from pseudorandom binary sequence bitstreams for three-connector channel example. From left to right: 0 to 20 ps of artificially introduced skew.

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IEEE802.3dj Work on 200 Gbps per Lane and How Different FEC Options Affect SI

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Broadcom Inc.

Recently, IEEE 802.3 has established 200 Gbps, 400 Gbps, 800 Gbps, and 1.6 Tbps Ethernet task force which is aiming at 200 Gbps per lane link rate. In order to study what is needed and has been adopted for the next speed node, this article covers new forward error correction (FEC) technology, modeling, and performance analysis to aim at 200+ Gbps Ethernet systems and how different FEC options affect signal integrity (SI).

With the fast growth of 5G/6G networks and AI/ML applications, the serial link data rates continuously increase due to high-speed communications and large bandwidth demands. Recently, IEEE 802.3 has established a 200 Gbps, 400 Gbps, 800 Gbps, and 1.6 Tbps Ethernet task force 802.3dj[4]. The new task force is aiming at 200 Gbps per lane link rate, doubled from 100 Gbps per lane as in IEEE 802.3bs[1] and 802.3ck[2].

A decade ago, industry successfully updated the signaling format from NRZ to PAM4 during the transition from 25 to 50 Gbps link rates. To offset the signal-to-noise ratio (SNR) penalty caused by higher modulation levels, FEC has become an essential part of the solution for PAM4 systems. This article is subsequent to two previous articles, "What is FEC and How Do I Use It?"[5] and "100+ Gbps Ethernet Forward Error Correction (FEC) Analysis)"[6], and provides updates for the next generation Ethernet rate, 200+ Gbps per lane.

To study what is needed and what has been adopted for the next speed node Ethernet, this article investigates different FEC schemes such as end-end, concatenated, and segmented FECs as well as their performance in different applications and the effect of different FEC schemes on SI.

Keeping up with the latest decision made within the IEEE 802.3dj task force for 800GBASE-R and 1.6TBASE-R, in which Hamming (128, 120) inner code has been adopted as a part of the FEC solution for 200 Gbps per lane IM-DD optics[7], concatenated FEC modeling and performance analysis became important to a multiple-part link system including a physical medium dependent (PMD) optical channel and two or more Attachment Unit Interface (AUI) electrical channels.

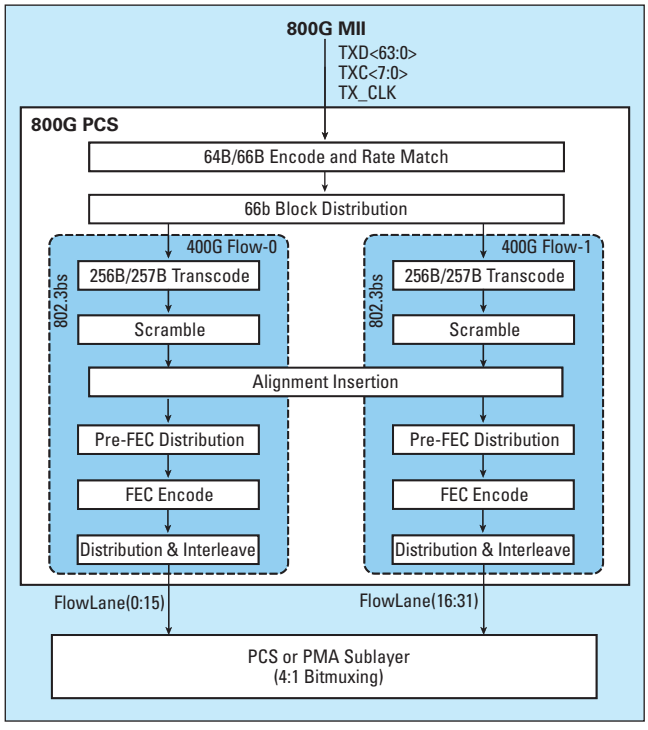


Fig. 1 800GE with 8×100G PHYs PCS transmitter flow.

Refreshed Channel Error Model and FEC Performance Analysis

In "100+ Gbp/s Ethernet Forward Error Correction (FEC) Analysis,"[6] random and burst channel errors and FEC performance analysis models were introduced for the 100 Gbps Ethernet rate. In this article, identical or similar models are used to study the next generation of FEC performance. In this section, we will add some updates based on the latest developments of the 802.3df[3] and 802.3dj[4] task forces.

FEC Architecture and Performance for 8×100G PHYs

Recently, the 802.3df task force adopted new Ethernet physical coding sublayer (PCS) and physical medium attachment (PMA) for 800GE with 8×100G PHYs, as shown in ***Figure 1***. It is based on two 400GE1 PCS FEC flows (flow-0 and flow-1) in parallel. In total, there are 32 flow lanes, each running at 25 Gbps. Specific flow lanes map to a given PMA output lane such that 4:1 bit multiplexing is conceptually the same as 400GE.

800GE with 8×100G PHYs has two flows, each contains two Reed Solomon (RS) (544, 514, 15) codewords. To utilize more coding gain, the 802.3df task force has decided to allow each physical lane to access all four FEC codewords equally, which results in 4-way codeword interleaving rather than 2-way codeword interleaving as in 802.3bs[1].

Figure 2 shows post-FEC FLR performances vs. slicer SNR values with 2-way and 4-way interleaving schemes, respectively. We can see that 4-way interleaving outperforms 2-way interleaving, especially for burst errors with α=0.75. Such analysis and contributions have helped the 802.3df task force adopt 4:1 bit multiplexing and 4-way codeword interleaving in its PCS/PMA specification.

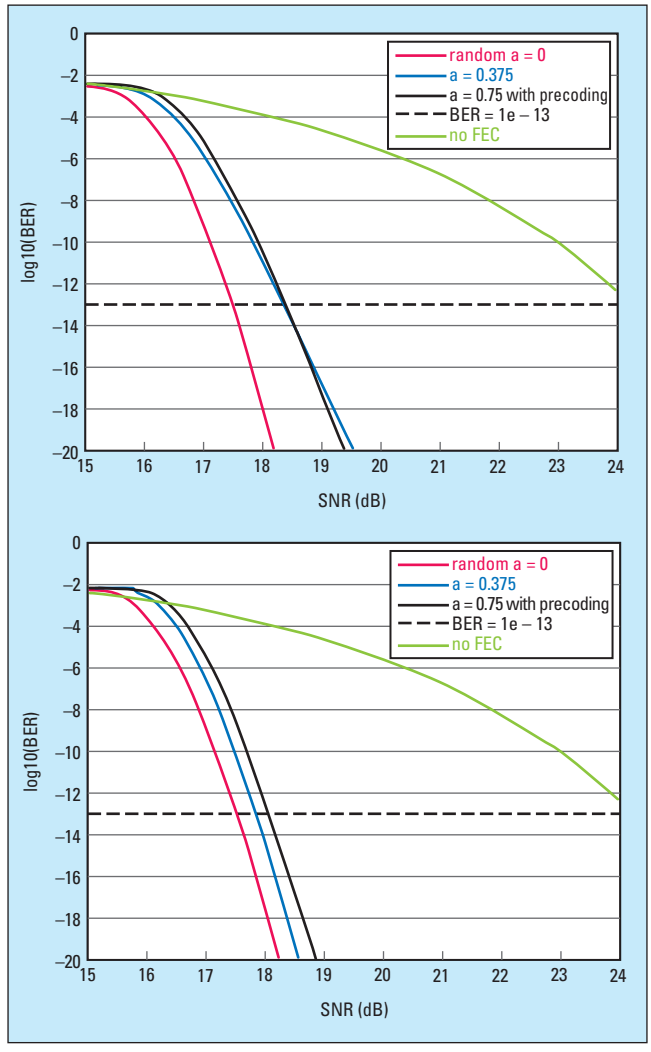


Fig. 2 Post-FEC BER performance vs. slicer SNR values for 4:1 bit multiplexing with 2-way (top) and 4-way (bottom) codeword interleaving coding schemes.

200 Gbps FEC Schemes and Coding Algorithms for Optical Channels

The 802.3dj task force has doubled the data rate from 100 to 200 Gbps per lane. In this section, we will study the potential FEC solutions for chip to optical module interfaces at 200 Gbps data rate, provide performance analysis for different coding schemes and coding algorithms, and discuss their effects on system SI.

Three FEC Architectures

There are three major FEC architectures in a multipart link system that have been discussed in the 802.3dj task force and shown in ***Figure 3***:

- Type-1: Single FEC spans multiple AUIs and the PMD link, referred to as "end-end FEC"
- Type-2: Outer FEC spans multiple AUIs and PMD link (like Type-1) with an additional inner FEC spans PMD link, referred to as "concatenated FEC"
- Type-3: Different FECs are dedicated to AUIs and PMD links, referred to as "terminated FEC."

200GBASE-R, 400GBASE-R, and 800GBASE-R with 100 Gbps per lane use Type-1 FEC, in which electrical

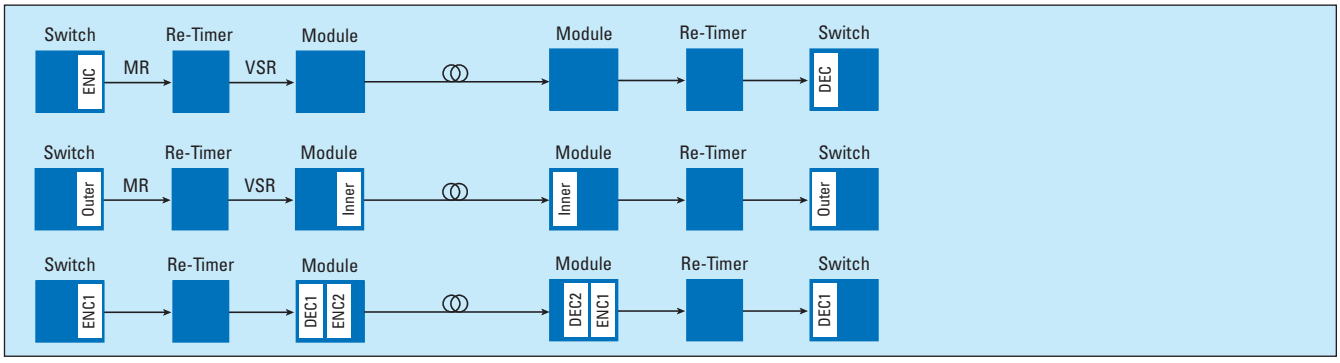


Fig. 3 Three types of FEC architectures (top: end-end; middle: concatenated; bottom: terminated).

TABLE 1

ALTERNATIVE RS CODES BESIDES RS (544, 514, 15) AND PERFORMANCE COMPARISONS

RS code (n, k, t)	*Bits per symbol*	*Code rate (k/n)*	*SNR (dB)*	*SER_{pam4}*
RS (544, 514, 15)	10	0.945	17.45	6.4e-4
RS (560, 514, 23)	10	0.918	16.74	1.6e-3
RS (576, 514, 31)	10	0.892	16.25	2.8e-3
RS (1088, 1028, 30)	12	0.945	17.02	1.1e-3
RS (2176, 2056, 60)	12	0.945	16.63	1.8e-3
RS (3264, 3084, 90)	12	0.945	16.46	2.2e-3
RS (4080, 3855, 112)	12	0.945	16.39	2.4e-3

AUIs and optical PMD link share a single FEC located at both ends of the hosts (such as switch chips). The performance analysis for such end-end FEC has been described in "100+ Gb/s Ethernet Forward Error Correction (FEC) Analysis"[6]. In order to meet the 1e-13 post-FEC BER target or the 6.2e-11 FLR target, the overall input BER to the end-end FEC needs to be 2.8e-4 or lower, with the combination of 2.4e-4 BER target for PMD link and 1e-5 BER target for AUI interfaces.

In order to double the data rate to 200+ Gbps per lane, the PMD link and/or AUIs might need extra FEC protection (further relaxing pre-FEC BER). Hence, both Type-2 and Type-3 FEC architectures are considered.

For Type-2 concatenated FEC, an outer FEC spans the whole link from host to host (like Type-1). An inner FEC spans only the PMD part. The inner FEC corrects most errors contributed by the PMD part, while the outer FEC corrects PMD errors not corrected by the inner FEC and errors contributed by the AUIs. The combined effect of inner and outer FECs results in the target BER and FLR for the whole link. This concatenated FEC scheme is new for 802.3.

For Type-3 segmented FEC, dedicated FECs protect different parts of the link such that DEC_1 corrects errors contributed only by one chip-module interface, while DEC_2 corrects error contributed only by PMD link. Since each part of the link has its own FEC protection, no BER target tradeoff between the AUIs and the PMD link is required. Both 400GBASE-ZR and 802.3cw use terminated FEC.

Compared to Type-1, both Type-2 and Type-3 might provide better coding gain to PMD link and/or AUIs. However, Type-3 FEC architecture expects extra latency, power, and complexity due to three FEC segments (three sets of encoders and decoders) to support. Type-2 FEC provides extra FEC protection for the PMD link with smaller increments in latency, power, and complexity compared to Type-3 FEC. The intent of Type-2 FEC is to provide a compromise which offers better performance than Type-1 and lower cost than Type-3. Therefore, Type-2 concatenated FEC has been adopted as a part of the FEC approach for 200 Gbps per lane IM-DD optics.[7] Details of the proposed concatenated FEC will be discussed later. In next section, the outer FEC at the host sides will be studied.

Host FEC

Upon transitioning from 100 to 200 Gbps per lane, industry and the 802.3dj task force still prefer to keep the similar PCS structure and RS FEC for maximum reuse and backward compatibility.

Alternative Options of PCS Reed Solomon (RS) Codes

To ease the system design, certain construction rules and assumptions are taken for PCS RS code selection. For each candidate RS (n, k, t) over GF (2^m)[8]:

- Each RS symbol consists of 8 to 12 bits (e.g., 10-bit symbol for KP-FEC, m=10)
- Assume 256B/257B block code to avoid additional transcoding
- Message size (m*k bits) corresponds to an integer

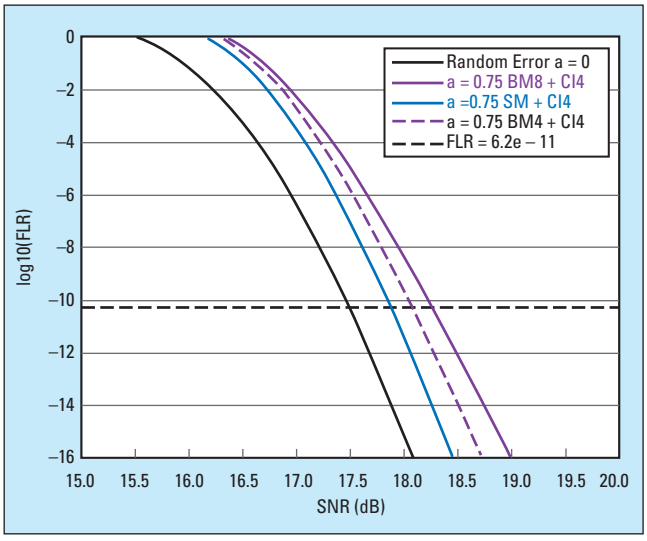


Fig. 4 FEC performance for random error a=0 and burst error a=0.75 with 4-way codeword interleaving.

number of 257-bit blocks
- Codeword spreads evenly across 4, 8, and 16 physical lanes
- Signaling rate is an integer multiple of a 625 MHz reference clock.

Table 1 lists a group of candidate RS codes that meet the above construction rules and assumptions. Their required slicer SNRs and SER_{pam4} to meet 1e-13 post-FEC BER are calculated for random error case (α=0, where "α" is the probability of getting an error in the next PAM4 symbol following an initial error). We can see that increasing error correction capacity t (number of RS symbol errors can be corrected per codeword) results in larger coding gain and relaxing pre-FEC BER target. For example, RS (576, 514, 31) and RS (4088, 3855, 112) codes can provide more than 1 dB coding gains over RS (544, 514, 15) code. However, the larger t value implies lower code rate and/or longer codeword length. Lowering code rate is undesirable for bandwidth limited copper channels such as backplane or copper cable channels. Meanwhile, the longer codeword length normally introduces larger latency and might not be suitable for systems with low latency requirement, such as AI and ML applications.

RS code encoder is a straightforward shift register[8] which contributes negligible encoding latency while the majority of coding latency is from the decoder. An RS code decoder has three stages:
- Syndrome generation: FEC codeword accumulation time at port speed
- Key equation solver: Berlecamp-Massey algorithm normally has 2 t iterations plus a few additional clock cycles
- Chien search and data correction: FEC codeword size and datapath width dependent

Table 2 lists the decoder latency for different FEC codes with selected numbers of physical lanes and codeword interleaving depths. RS (544, 514, 15) FEC with 4-way codeword interleaving over 4×200G PHYs introduces ~55 ns latency.

It is likely that the 802.3dj task force will reuse RS (544, 514, 15) (also known as the KP-FEC) as PCS FEC code due to its backward compatibility and tradeoff between performance and latency.

Symbol Multiplexing and 4-way Codeword Interleaving Scheme

Analysis in "100+ Gb/s Ethernet Forward Error Correction (FEC) Analysis"[6] showed that 4:1 bit multiplexing has larger coding gain penalty for burst errors than 2:1 bit multiplexing and symbol multiplexing. We can expect that increasing the bit multiplexing to 8:1 for 200 Gbps per lane will further degrade the performance.

To avoid bit-multiplexing penalty, symbol multiplexing is considered. It is not surprising to see in ***Figure 4*** that SM+CI4 outperforms BM4 and BM8 for burst error case α=0.75 and reduces the gap to random error case α=0.

It is likely that the 802.3dj task force will adopt RS (544, 514, 15) with symbol multiplexing and 4-way codeword interleaving as its host PCS and PMA coding scheme.

Concatenated FEC: Inner Code and Decoding Algorithms for the Optical PMD

In this section, we will focus on Type-2 concatenated FEC, which has been adopted by 802.3dj as a part of the FEC approach for 200 Gbps per lane IM-DD optics.[7]

TABLE 2

RS CODE DECODER LATENCY

RS FEC (n, k, t)	Link rate (Gbps)	Cycle time (GHz)	Codeword interleaving	Physical lanes per port	Stage 1 latency (ns)	Stage 2 latency (ns)	Stage 3 latency (ns)	Total latency (ns)
RS (544, 514, 15)	106.25	1.56	1	1	51.20	21.12	8.64	80.96
RS (544, 514, 15)	212.5	1.56	1	1	25.60	21.12	8.64	55.36
RS (544, 514, 15)	212.5	1.56	1	4	6.40	21.12	8.64	36.16
RS (544, 514, 15)	212.5	1.56	4	4	25.6	21.12	8.64	55.36
RS (576, 514, 31)	225	1.56	1	4	6.40	41.60	8.96	56.96
RS (1088, 1028, 30)	212.5	1.56	1	4	15.36	40.32	16.26	71.94
RS (2176, 2056, 60)	212.5	1.56	1	4	30.72	78.72	29.31	138.75
RS (3264, 3084, 90)	212.5	1.56	1	4	46.08	117.12	42.37	205.57
RS (4080, 3855, 112)	212.5	1.56	1	4	57.60	145.28	52.16	255.04

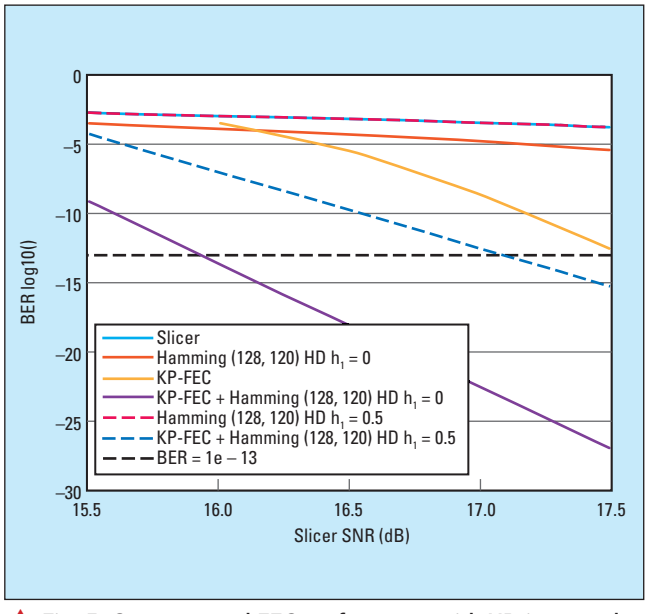


Fig. 5 Concatenated FEC performance with HD inner code decoding.

Hamming Code and its Encoder

For a concatenated FEC, the inner code should be short and with small overhead, such that the overall concatenated FEC has reasonable code rate and relatively low latency. Hence, Hamming codes or BCH codes[8] have been considered.

Recently, the 802.3dj task force adopted Hamming (n=128, k=120) code as its inner code of the concatenated FEC. This inner code is based on the Hamming code (127, 120) by adding one extended parity check bit.

Due to the extended parity check bit, the minimum distance d_{min}=4. It will improve the error detection capability to 3 bits per codeword while the error correction capability is still 1 bit per codeword.

The encoding process of a linear block code or a Hamming code can be defined as a matrix operation: $c=u \cdot G_{k,n}$, where c is the codeword sequence, u is the information part of the codeword, and G is the generator matrix that uniquely defines the linear block code.

Hamming Code Decoder

The decoding procedure for a Hamming code consists of three steps:

1. Compute the syndrome sequence s of the received vector r to detect errors
2. Identify the location of the error
3. Correct the error.

In the first step, the syndrome sequence s is calculated as:

$$s = H_{n\text{-}k,n} \cdot r$$

where r is received noisy sequence and H is the parity check matrix paired with the generator matrix G.

If syndrome sequence s is all-zero, a correct transmission is assumed. Otherwise, errors are detected. For Hamming code (128, 120) with d_{min} = 4, it is able to detect up to three bits in error per codeword.

The second step of the decoding is generally the hardest part, to identify the error location. For a Hamming code with d_{min} = 4, it can only correct one bit error per codeword. Since there are eight bits in the syndrome sequence $s = (s_0, s_1, s_2, s_3, s_4, s_5, s_6, s_7)$ and s_0 is the extended parity bit, there are 2^7 possible patterns of $s' = (s_1, s_2, s_3, s_4, s_5, s_6, s_7)$. For a hard decision decoding decoder, each of these s' corresponds to a unique error location in r. After the error location is identified, the error can be corrected easily.

If there are more than 1 bit errors per codeword, such a decoding procedure could detect errors but miscorrect them in wrong locations, referred to as micorrection. For concatenated codes, miscorrections are highly undesirable because they introduce additional errors (on top of channel errors) into the outer code decoding and sometimes make outer code decoder even harder to correct those miscorrections. For Hamming code (128, 120), the probability of miscorrection is as high as 0.5039 and not negligible. ***Figure 5*** shows concatenated FEC performance with hard decision (HD) decoding for different channel error profiles, with DFE coefficients of h_1=0 and h_1=0.5. We can see that for random error case (h_1=0), the inner code can improve slicer BER 1-2 order of magnitude and improve post-FEC BER 5-10 order of magnitude over KP-FEC only, equivalent to 1.5 dB coding gain to meet 1e-13 post-FEC BER. However, for correlated error case (h_1=0.5), the performance of the concatenated FEC with HD inner code decoding degrades significantly due to the miscorrections. The coding gain reduces to only 0.3 dB.

In order to mitigate the inner code miscorrection impact and improve the concatenated FEC performance, soft decision (SD) decoding algorithms and further interleaving schemes can be considered.

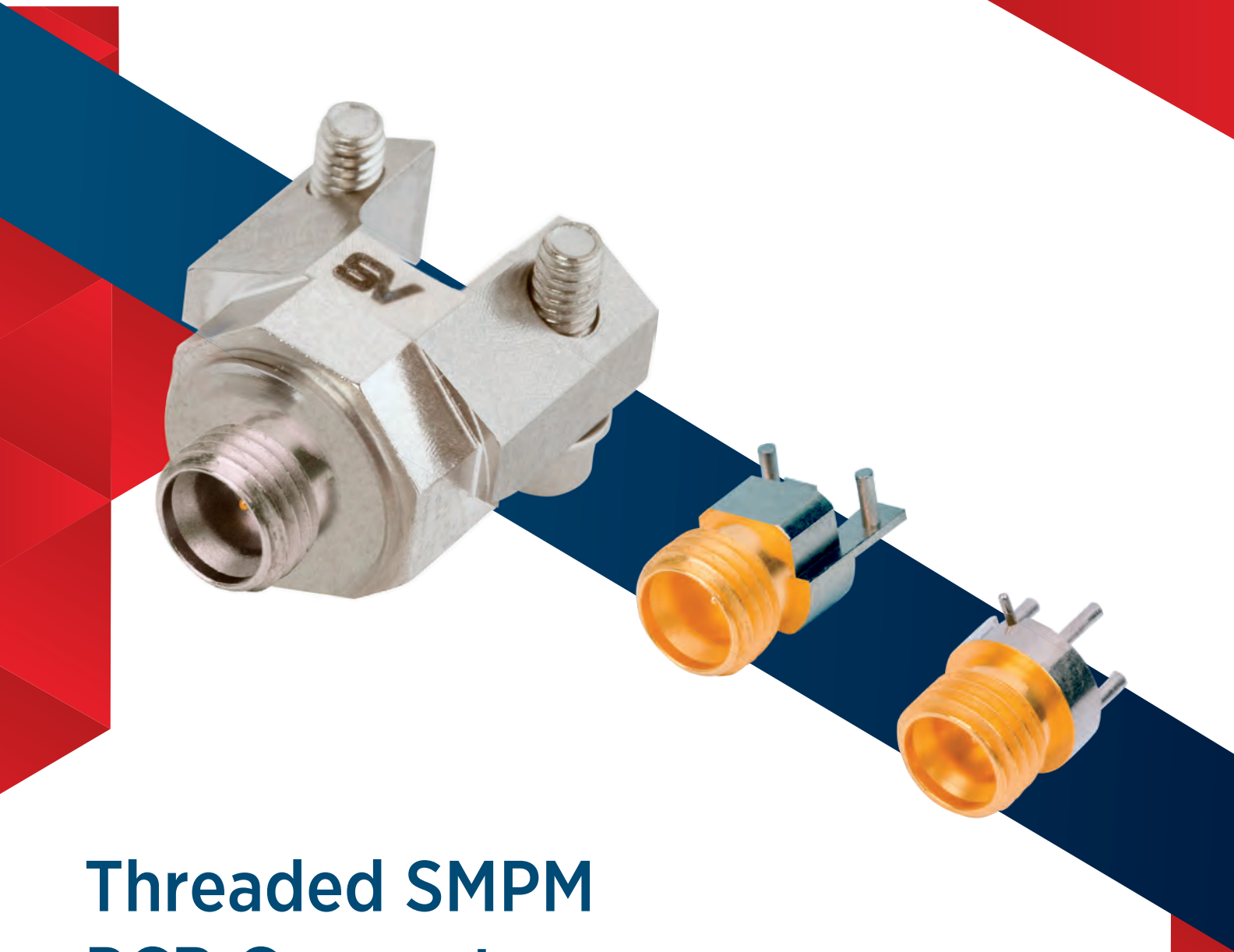
Soft Decision Decoding

If the outputs of the receiver are unquantized or quantized into more than two levels, a sequence of soft decision input can be taken to the decoder to process SD decoding.

Because the decoder uses the additional information to recover the transmitted codeword, SD decoding provides better FEC performance than hard decision decoding. In general, SD maximum likelihood decoding (MLD) of a code has about 3 dB of coding gain over HD decoding.[8] However, MLD can be much harder to implement than HD decoding and requires more computational complexity and decoding latency.

To achieve a better trade-off between performance and decoding complexity, some practical suboptimal soft-decoding algorithms can be applied. Chase introduced three algorithms in "A Class of Algorithms for Decoding Block Codes with Channel Measurement Information"[9], namely, algorithm-1, algorithm-2, and algorithm-3, with different levels of complexity. This article uses Chase's algorithm-2 as the SD decoding algorithm for the inner Hamming decoder.

Let $r = (r_0, r_1, \ldots, r_{63})$ be a SD received sequence at the output of the receiver slicer. Each receiver symbol r_i with $0 \le i \le 63$, is decided independently to z_i, $z_i \in \{0, 1, 2, 3\}$ for PAM4 signaling. Then, the magnitude of slicer



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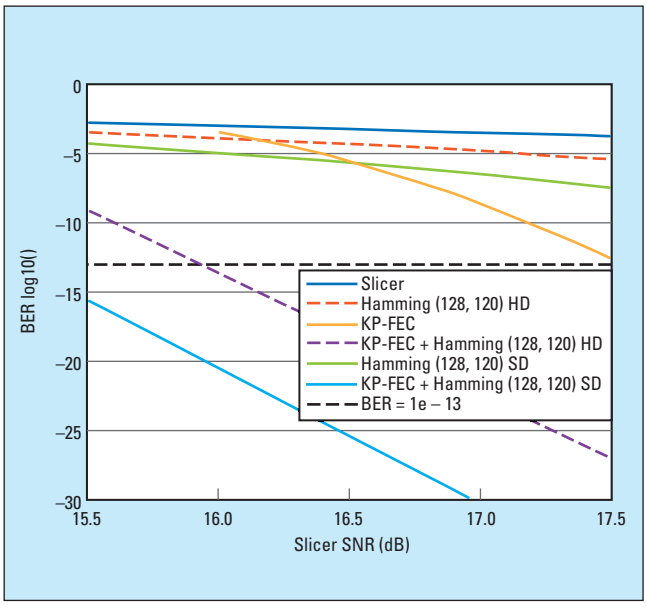


Fig. 6 Concatenated FEC performance with HD and SD inner code decodings for h_1=0.

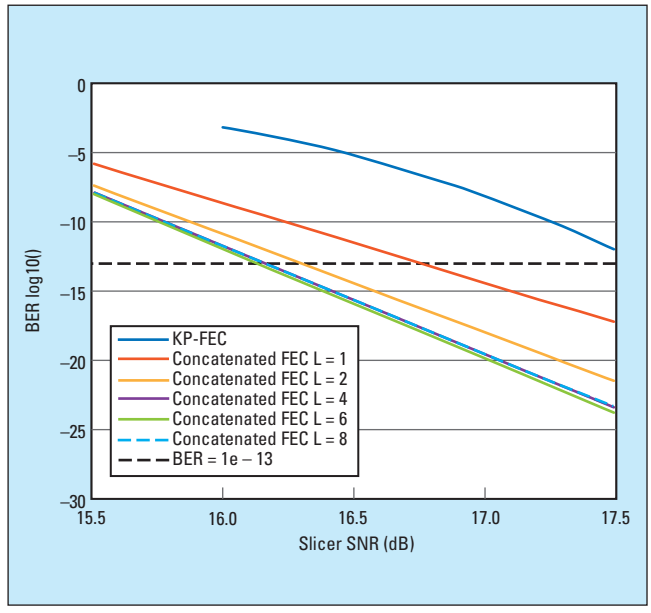


Fig. 7 Concatenated FEC performance with channel block interleaving for h_1=0.5.

error, $|r_i - z_i|$, can be used as a reliability measure of the HD decoded bit z_i. The larger $|r_i - z_i|$ is, the HD z_i becomes less reliable. Based on the reliability measure of the received symbols, a group of least reliable positions (LRPs) can be identified. The precision of the slicer errors is implementation determined. 5-bit fixed-point values are used in this article for the slicer error, $|r_i - z_i|$.

In Chase's algorithm-2, the number of LRP locations to consider is $[d_{min}/2]$. In our case, d_{min}=4 for Hamming code (128, 120). Hence, there are 2^2 possible test patterns, including the all-zero pattern. The decoding procedure is in following steps:

1. Form the HD received sequence z from r and assign a reliability value to each symbol of z
2. Generate the error patterns in E one at a time, possible in likelihood order. For each error pattern e in E, form the test patterns z+e
3. Decode each test pattern into a codeword using HD decoder
4. Compute the soft decision decoding metric for each generated candidate codeword
5. Select the candidate codeword with the best metric as the coded solution.

There are different ways to compute SD decoding metric for each generated candidate codeword. As an example, we can add slicer errors of selected LRPs in each test pattern and corresponding HD corrected position. The larger the summation value, the more likely the generated codeword candidate is.

Figure 6 shows concatenated FEC performance with HD and SD inner code decodings for random error case h_1=0. We can see that SD decoding outperforms HD decoding. SD decoding can improve slicer BER 2-3 order of magnitude and provide more than 2 dB coding gain to meet 1e-13 post-FEC BER compared with KP-FEC only.

To improve the concatenated FEC performance, especially over burst channel errors, further interleaving schemes within PMD inner code sublayer are proposed.

Inner Code Interleaving Schemes

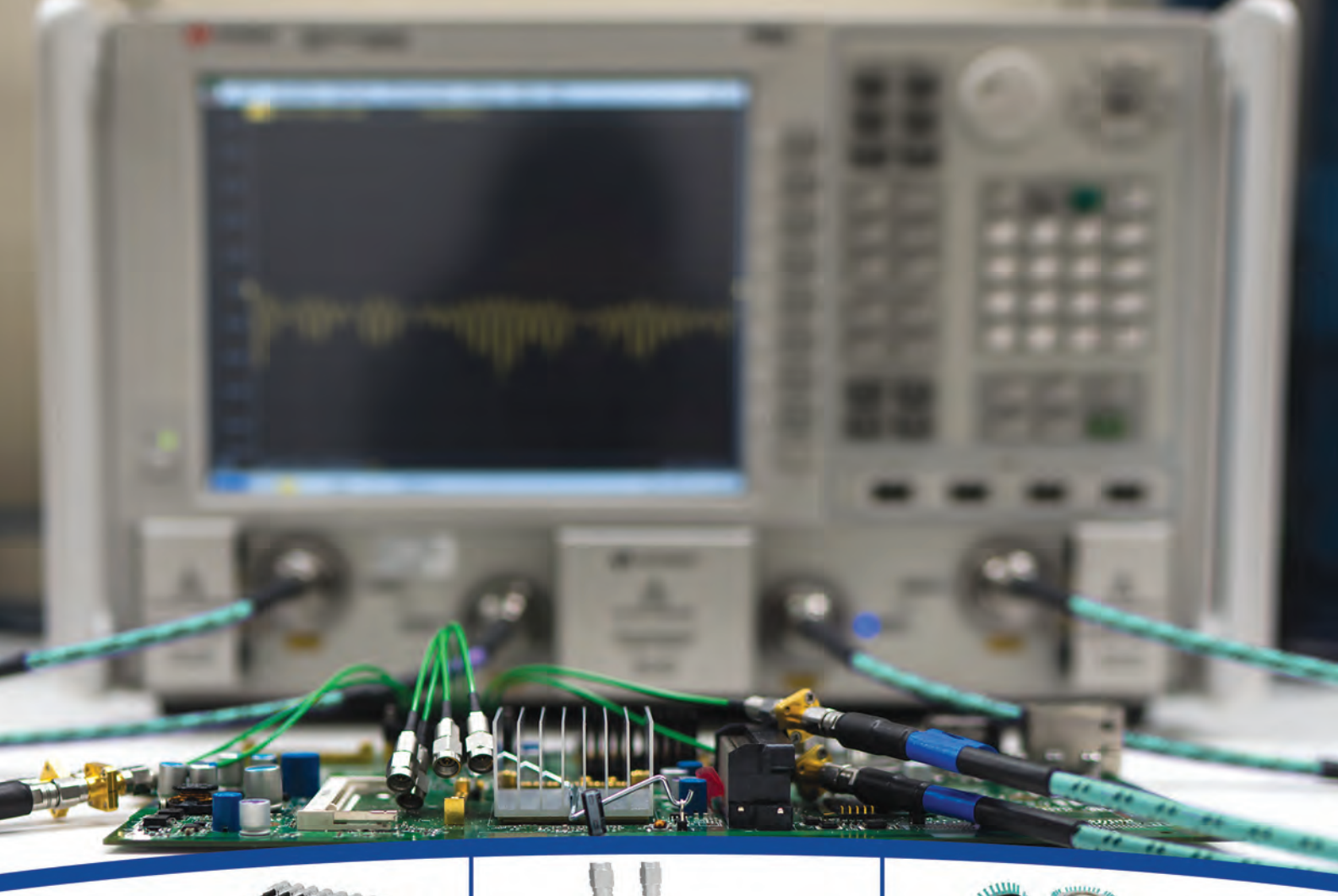
First, we can consider a block interleaver between PMD channel and inner Hamming code (128, 120). It simply arranges L Hamming inner codes into L rows of a rectangular block and then transmitting/receiving the block column by column. Even though the minimum distance of the interleaved block is still d_{min}=4 as an individual Hamming code (128, 120), this channel block interleaving can break a long burst PAM4 error into L different codewords.

By doing this, we expect that the concatenated code with channel block interleaving can tolerate longer burst errors or more DFE error propagation. ***Figure 7*** shows the concatenated FEC performance with channel block interleaving of L=1, 2 ... and up to 8 for h_1=0.5. We can see that with L > 4 the channel interleaving improves concatenated coding gain about 1.5 dB over KP-FEC only.

To break the long burst errors and improve concatenated code performance, there are multiple interleaving schemes proposed in FEC baseline proposal for 200 Gbps per Lane IM-DD Optical PMDs[7]:

- Hamming interleaver L=8 to break the long burst errors into different inner codewords
- Circular shift block maximizes the distance in bauds between transmitted PAM4 symbols from two different RS symbols in the same RS(544, 514, 15) outer code
- Convolutional interleaver guarantees that the 12 x 10 bit payload of the Hamming encoder comes from 12 distinct RS codewords

The proposal FEC baseline proposal for 200 Gbps per Lane IM-DD Optical PMDs[7] describes the above three interleaving functions. The proposal claims that the inner Hamming code (128, 120) with the above three interleaving functions could relax the PMD optical BER target from 2.4e-4 to 4.8e-3, more than one order of magnitude.



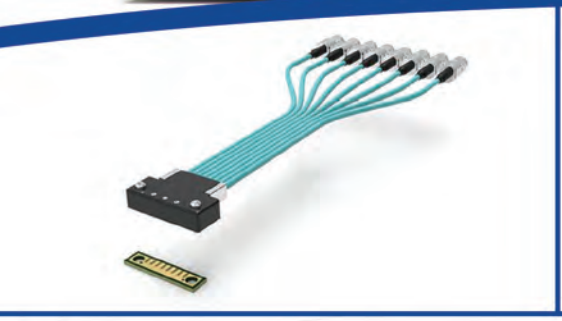


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TABLE 3

REQUIRED SLICER SNR FOR DIFFERENT BER TARGETS FOR PAM4 OVER AWGN CHANNEL

BER Targets	1e-13	1e-6	1e-5	1e-4	2.4e-4	4.8e-3
SNR (dB)	24.3	20.4	19.5	18.2	17.7	14.9

However, the major cost of adding inner code is the latency, especially with the convolutional interleaver. The latency of inner code itself, including encoder and decoding, is about 10 ns, while the convolutional interleaver for 800GBASE-R with 4-way RS codeword interleaving increases the latency to 56 ns. For 800GBASE-R/400GBASE-R with 2-way RS codeword interleaving, the latency could be further increased to 140 ns.

Low Latency PMD PHY

To cut the latency for a shorter distance of the PMD optical channel or better optic modules, two different FEC modes have been discussed and proposed to the 802.3dj task force:

- Mode_FECo: Optical link runs with RS (544, 514, 15) FEC protection alone, the same as end-end FEC
- Mode_FECi: Optical link runs with RS (544, 514, 15) FEC protection operating as an outer code, supplemented by Hamming code (128,120) protection operating as an inner code.

Of course, the PMD BER target would be different for these two FEC modes, provided that the error statistics are sufficiently random:

- Mode_FECo: The BER of the PMD link shall be less than 2.4e-4 when processed with an 800GBASE-R/1.6TBASE-R PCS
- Mode_FECi: The BER of the PMD link shall be less than 4.8e-3 when processed with an 800GBASE-R/1.6TBASE-R PCS and an inner code sublayer.

Basically, we need two separate PHY specifications. One is associated with Mode_FECi for optical channels longer than 2 km, and the other is associated with Mode_FECo for either short reach (say less than 500 m) or co-packaged optic (CPO) and linear pluggable optic (LPO) type of interfaces.

How Do FEC Options Affect System Signal Integrity?

From the discussions and analysis presented, we can conclude that different FEC options provide different coding gains with varying levels of cost, including coding overhead, coding latency, and complexity. Those factors will affect system signal integrity through different aspects.

First, FEC can relax host SerDes BER target. The larger coding gain the FEC provides, the lower the BER target can be relaxed. For example, FEC baseline proposal for 200 Gbps per lane IM-DD Optical PMDs[7] claims that the proposed concatenated code can relax PHY's BER target from 2.4e-4 to 4.8e-3 for 200 Gbps. ***Table 3*** lists the required slicer SNR for different BER targets for PAM4 signaling format over AWGN channel. Relaxing SerDes BER is equivalent to tolerating more noise, crosstalk, and jitter. Without increasing signal energy or equalization power, the proposed concatenated FEC can help us tolerate 2.8 dB more noise, jitter, crosstalk, or combined.

Second, strong interleaving schemes at host PCS or/and PMD inner code sublayers can effectively mitigate DFE error propagation, low frequency jitter, baseline wander, and other sources of correlated errors.

Of course, such high coding gain and long burst error tolerance of certain FEC options have inevitable cost. The proposed concatenated FEC provides up to 2.8 dB coding gain to the PMD link, but increases more than 6.7% link rate and more than 50 ns latency. The increased link rate could introduce significantly higher channel loss and crosstalk for a bandwidth limited channel. The increased latency could make the FEC option unsuitable to AI and ML applications in which a low latency requirement is critical.

Last but not least, the interoperability between different PHYs with different FEC options and FEC modes are desirable. The 802.3dj task force is developing the specifications to ensure such interoperability.

Conclusion

In this article, channel error models and FEC performance analysis have been updated according to industry changes. Different Ethernet coding schemes have been studied and simulated for 800GE and 1.6GE systems with 200 Gbps per lane. Concatenated FEC with soft-decision decoding for inner code to protect 200 Gbps optical link is investigated. The effect of different FEC options on system SI is discussed as well.

REFERENCES

1. IEEE Std 802.3bs-2017 IEEE Standard for Ethernet: Media Access Control Parameters, Physical Layers and Management Parameters for 200 Gb/s and 400 Gb/s Operation.
2. IEEE Std 802.3ck-2022 IEEE Standard for Ethernet: Physical Layer Specifications and Management Parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Based on 100 Gb/s Signaling.
3. IEEE P802.3df 400 Gb/s and 800 Gb/s Ethernet Task Force, https://www.ieee802.org/3/df/index.html.
4. IEEE P802.3dj 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet Task Force, https://www.ieee802.org/3/dj/index.html.
5. C. Liu, "What is FEC, and How Do I Use It?" *Signal Integrity Journal*, https://www.signalintegrityjournal.com/articles/1284-what-is-fec-and-how-do-i-use-it.
6. C. Liu, "100+ Gb/s Ethernet Forward Error Correction (FEC) Analysis," *DesignCon 2019*.
7. L. Patra, A. Farhood, R. Radhamohan, W. Bliss, S. Ramesh, and D. Cassan, "FEC Baseline Proposal for 200 Gbps per Lane IM-DD Optical PMDs," IEEE P802.3dj Task Force, March 2023, https://www.ieee802.org/3/dj/public/23_03/patra_3dj_01b_2303.pdf.
8. S. Lin and D. Costello, Error Control Coding, *Prentice Hall*, February 2002.
9. D. Chase, "A Class of Algorithms for Decoding Block Codes with Channel Measurement Information", *IEEE Trans. on Information Theory*, Vol. IT-18, No. 1, January 1972.

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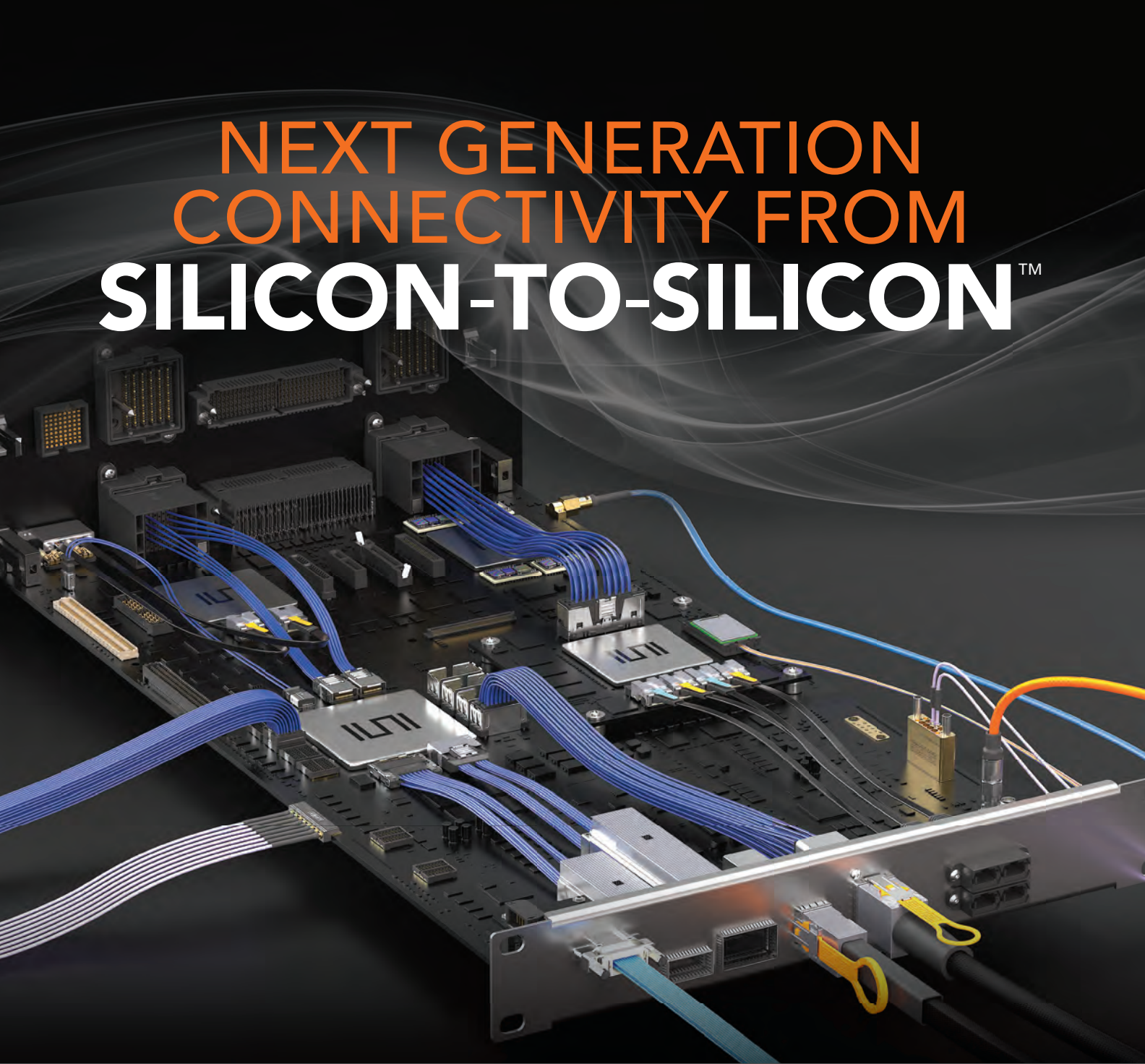

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PCB Laminate Anisotropy: The Impact on Advanced Via Modeling

Bert Simonovich
Lamsim Enterprises, Stittsville, Ontario, Canada

As artificial intelligence (AI) and machine learning (ML) challenge engineers to process more data faster, electronic design automation (EDA) tools are progressively integrating AI and ML to advance the design process. Many refer to this process as "shifting-left" or "shift-left."

Several EDA tools often boast about their capability to extract and simulate nets from a PCB design file with a simple click of a button. However, if the user is not cognizant of dielectric anisotropy, or if the software does not account for it, the simulation results may be inaccurate. This could pose a challenge for simulating the next generation 112/224 Gbps interconnect due to the shrinking of already tight margins.

In the process of modeling a PCB via, it is crucial to obtain accurate dielectric material properties from reliable sources. A key factor in this regard is relative permittivity, or dielectric constant (Dk).

Copper clad laminate (CCL) panels used for PCB fabrication are a mixture of fiberglass and resin, cladded on one or both sides with copper. CCL suppliers use various test methods to determine Dk and dissipation factor (Df), which are eventually published in their construction tables. PCB fabricators and signal integrity (SI) and power integrity (PI) engineers then rely on these values, which are used to design PCB stackups and perform SI/PI analysis.

There are over a dozen test methods specified in Institute of Printed Circuits (IPC) specifications. These test methods were designed as a means of testing for quality control in a production environment and do not guarantee the numbers are accurate for design applications. Usually, CCL suppliers include a footnote disclaimer with similar wording to that effect in their construction tables.

PCB Laminate Anisotropy

All glass weave reinforced laminates are anisotropic, meaning dielectric properties will be different along different axes. Unfortunately, the publication of Dk by CCL suppliers does not include anisotropic properties required for precise impedance prediction and SI modeling.

The values of Dk can be different based on the specific test method used. Some methods give results from in-plane measurements, where the electric fields are parallel to the test sample. Conversely, other methods derive Dk from out-of-plane

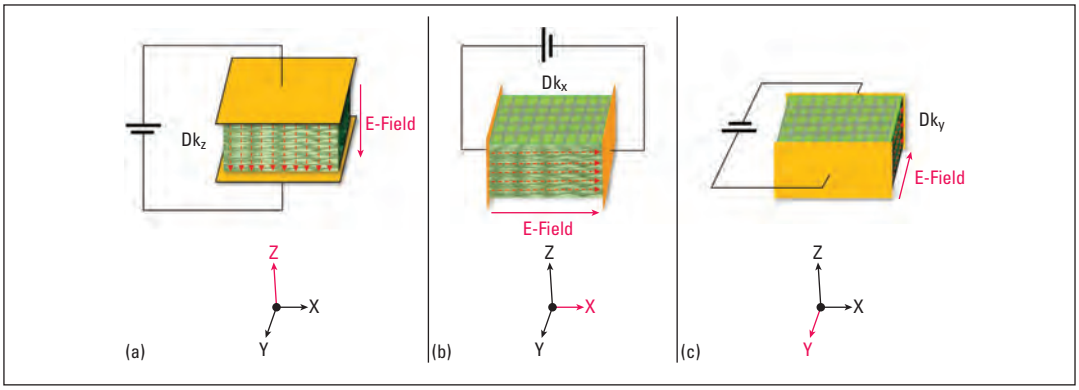


Fig. 1 E-field orientation relative to the glass weave reinforcement in PCB laminates when a DC electrical potential is applied: E-fields are out-of-plane with respect to the glass weave (a) and in-plane with the glass weave (b, c).

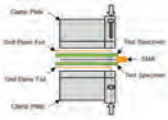
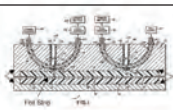
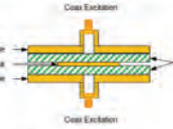
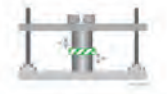
	Test Method	E-Field In-Plane (Dk_{xy})	E-Field Out-of-Plane (Dk_z)
	Clamped Stripline Resonator Ref: IPC-TM-650 2.5.5.5 RevC		✓
	Bereskin Stripline Resonator Ref: Patent US5187, 443 Feb. 16, 1993		✓
	Balanced-Type Circular Disk Resonator Ref: IEC 63185:2020		✓
	Split-Cylinder Resonator Ref: IPC-TM-650 2.5.5.13	✓	
	Split-Post Dielectric Resonator (a.k.a. Split-Post Cavity)	✓	

Fig. 2 Comparative table of E-field orientation and resulting Dk_{xy} or Dk_z across popular test methods employed by CCL suppliers.

measurements, where the electric fields are perpendicular to the test sample.

Figure 1a shows a block of fiberglass reinforced laminate, with the glass weave and copper plates running parallel to the x-y axis. When a DC potential is applied, a uniform electric field is out-of-plane in the z-direction, thereby creating a capacitor. Since the effective Dk is the ratio of actual structure's capacitance, to the capacitance when the dielectric is replaced by air, we denote this ratio as Dk_z.

Figure 1b and ***1c*** show that when the conducting plates are placed perpendicular to the direction of the glass weave, the E-fields align with the x or y axis and are in-plane. Even though there might be slight variations in the effective Dk in these directions, heuristically we assume they are equal and refer to them as Dk_{xy}.

Depending on the test method used, Dk measured may be different due to the test fixture's generated E-field orientation relative to the glass weave. ***Figure 2*** summarizes E-field orientation when compared against popular test methods used by CCL suppliers. Dk obtained by these test methods are denoted as in-plane (Dk_{xy}) or out-of-plane (Dk_z).

Dk_{xy} is typically higher compared to Dk_z, depending on the glass resin mixtures of the sample tested as shown in ***Figure 3a***. The rules of solid mixtures[1] can be used to estimate anisotropy of the glass and resin mixture. If the E-field is polarized in the z-direction, using a Dk of 6.8 for E-glass (Dk_g), a Dk of 2.5 for resin (Dk_r), volume fraction of resin (v_{resin} = 0.7), and volume fraction of E-glass (v_{glass} = 0.3), then the effective capacitance of each block is in series and Dk_z is determined to be 3.09, using the parallel mixing rule defined by:

$$Dk_z = \left[v_{resin} / Dk_r + v_{glass} / Dk_g \right]^{-1} = \left[0.7 / 2.5 + 0.3 / 6.8 \right]^{-1} = 3.09 \quad (1)$$

When the conductor plates are moved, as shown in ***Figure 3b***, and the mixture is polarized such that the E-field is parallel to the x-y axis, then the effective capacitance is in parallel and Dk_{xy} is determined to be 3.79, using the series mixing rule defined by:

$$Dk_{xy} = v_{resin} \cdot Dk_r + v_{glass} \cdot Dk_g = 0.7 \cdot 2.5 + 0.3 \cdot 6.8 = 3.79 \quad (2)$$

Using Equation 3, Anisotropy (Λ) of the mixture reveals that Dk_{xy} is 23% higher than Dk_z.

$$\Lambda = \left(\frac{Dk_{xy}}{Dk_z} - 1 \right) 100 = \left(\frac{3.79}{3.09} - 1 \right) 100 = 23\% \quad (3)$$

Anisotropy Implications for Via Modeling

PCB transmission lines run parallel to the glass weave and E-fields are predominantly out-of-plane. Thus, Dk_z is needed for accurate impedance modeling. Using Dk_{xy} instead means the impedance predicted from the field solver will be lower than what would be measured if the board was made exactly as specified in the stackup.

In the case of modeling vias, it gets more complicated. In ***Figure 4***, given a cross-section view of a typical via and stub, we observe the E-fields as the signal propagates, from left to right, along the microstrip transmission line on the top layer, through the via to an inner

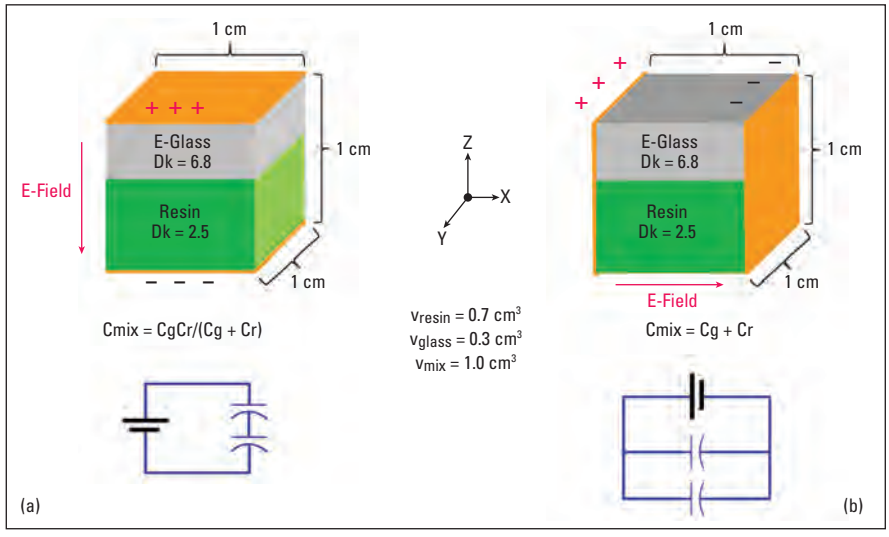


Fig. 3 Rule of solid mixtures: Parallel mixing rule is used when E-fields are polarized in Z-direction (a) and series mixing rule is used when E-fields are polarized in x-y direction (b).

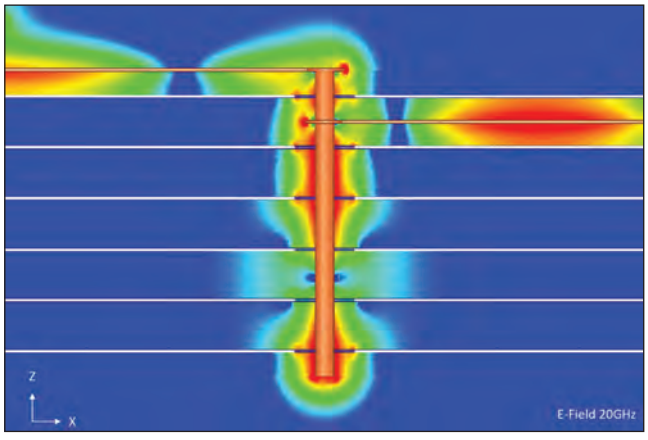


Fig. 4 Cross-section view of E-fields as a 20 GHz signal propagates from the microstrip top layer through a via with stub to a stripline layer 3 (HFSS simulation courtesy of Juliano Mologni, Ansys[4]).

stripline layer 3 and continuing through the stub.

Using the same value for Dk when modeling transmission lines and vias leads to inaccurate results for one or the other. If the CCL supplier's published numbers are out-of-plane, Dk_z, then the impedance for transmission lines will be correct, while the via impedance will end up being lower than modeled. On the other hand, if the published numbers are in-plane, Dk_{xy}, then the via impedance will be correct and the transmission line impedance will end up being higher.

Furthermore, using the wrong Dk for modeling via stubs will result in poor simulation correlation to measurements[2] and potentially the loss of channel margin due to maximum stub length guidelines based on simulation analysis.[3] This can be problematic for 112/224 Gbps interconnects by reducing already tight margins.

Figure 5 shows an example of this issue. A 26 mil (0.66 mm) pitch differential via with a 10 mil (0.254 mm) stub model was created in Keysight ADS[5] via designer (see ***Figure 5a***). A Dk_z of 3.09 and Dk_{xy} of 3.79 from Equation 1 and Equation 2 were used in the model for comparisons. After finite element method (FEM) simulation, S-parameters were saved in touchstone format and simulated in the circuit schematic shown in ***Figure 5b***.

Figure 5c compares differential insertion loss (IL) and return loss (RL) and ***Figure 5d*** compares differential time domain reflectometer (TDR) impedance. The red plots are using out-of-plane Dk_z and the blue plots are using in-plane Dk_{xy}. As can be seen, when out-of-plane Dk_z value is used in the model, it underestimates IL and impedance by approximately 8 Ohm. For 112 Gbps, the difference in loss at 28 GHz Nyquist frequency is ~ 0.3 dB. At 56 GHz Nyquist for 224 Gbps, the delta is ~ 0.9 dB, caused by the difference in stub resonant nulls at 106 and 95 GHz.

But this doesn't tell the whole story. While it is widely known that short, highly reflective channels can negatively impact channel performance, the issue has been exacerbated by the introduction of 4-level pulse amplitude modulated (PAM4) signaling, which reduces the signal-noise ratio by 9.5 dB. As bit rates continue to increase exponentially, traditional IL/RL masks and eye diagrams are no longer sufficient for assessing channel quality.

Channel operating margin (COM)[7] is a system-level metric approach adopted by the IEEE 802.3ck standard to validate the performance of a serial link. As part of COM, there is an effective return loss (ERL) metric that factors in reflections caused by impedance mismatches at the pins of the transmitter, receiver, and any other discontinuities between them. Thus, COM can be used to assess the impact of Dk anisotropy on key metrics.

A short channel representing a typical chip-to-chip (C2C) topology was modeled by concatenating touchstone files for vias and transmission lines using Keysight ADS[5], as depicted in ***Figure 6b***. The 2 in. (5.08 cm), 100 Ohm differential transmission line was modeled with Polar SI9000[6] using an out-of-plane Dk_z value of 3.09.

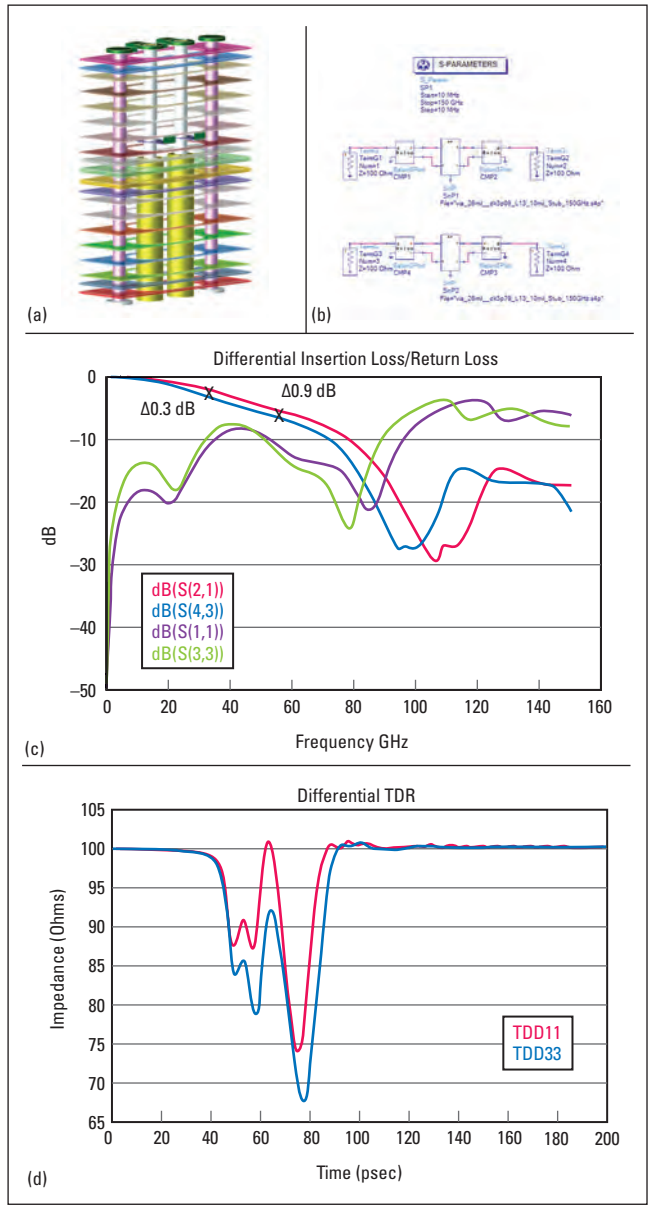


Fig. 5 Simulated results for differential IL/RL (c) and TDR impedance (d) of a differential via model with 10 mil (0.254 mm) stub using Dk_z of 3.09 (red plots) and Dk_{xy} of 3.79 (blue plots) for laminate. Modeled and simulated with Keysight ADS[5] via designer.

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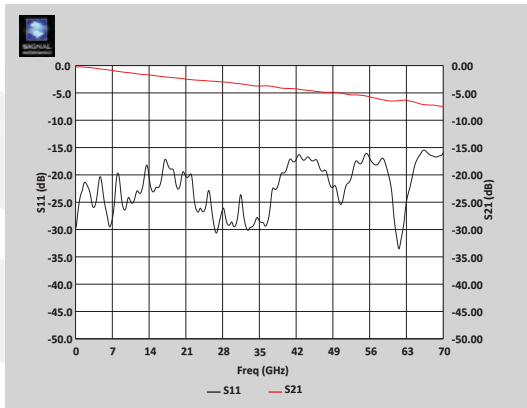

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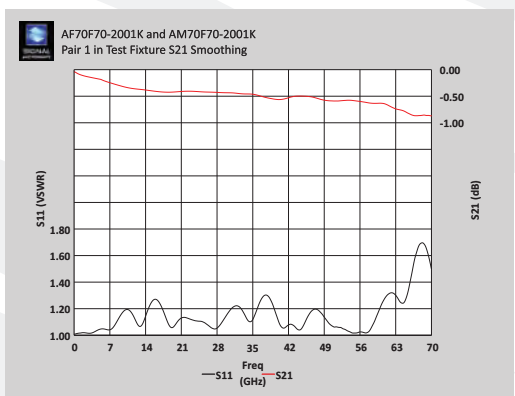

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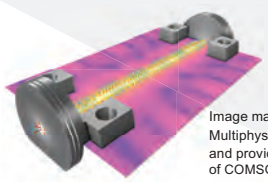

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Figure 6a shows the differential TDR response obtained using a Dk_z value of 3.09 for the via and transmission line models. As shown in ***Figure 6d***, both COM and ERL passed when a short package model was used. When the via files were replaced with files modeled with Dk_{xy} of 3.79, the differential TDR response is degraded, as shown in ***Figure 6c***. ***Figure 6e*** shows that although COM passed, it had reduced margins and ERL failed.

Of course, this was an extreme example with high Dk anisotropy. Choosing a dielectric with low Dk glass and higher resin content would improve the results. But if you have a tight loss budget to begin with, using the wrong numbers could cause failure to meet compliance once your board is built and tested.

Summary

Since woven glass PCB substrates are anisotropic, EDA design and modeling software hoping to advance AI and ML algorithms should have provisions to model anisotropic material, especially via transitions.

It is important to have awareness of the test method used by CCL suppliers for accurate modeling and simulation. Using out-of-plane Dk_z values instead of in-plane Dk_{xy} values for via modeling can cause misleading simulation results, which may result in reduced margins and potential compliance test failures when the design is built and tested.

It is recommended that CCL suppliers provide anisotropic properties in their Dk/Df construction tables. In lieu of that, my DesignCon 2024 paper and presentation titled "A Heuristic Approach to Assess Anisotropic Properties of Glass-reinforced PCB Substrates" will be delving deeper into anisotropy to reveal how to calculate anisotropy from CCL suppliers' Dk/Df construction tables. The full paper will be made available following the event. It will also be available on the Signal Integrity Journal website in late 2024.

REFERENCES

1. P. S. Neelakanta, "Handbook of Electromagnetic Materials: Monolithic and Composite Versions and Their Applications," *CRC Press LLC*, 1995.
2. L. Simonovich, E. Bogatin, and Y. Cao, "Differential Via Modeling Methodology," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, Vol. 1, No. 5, pp. 722–730, May 2011, doi: 10.1109/TCPMT.2010.2103313.
3. B. Simonovich, "Via Stubs – Are They all Bad?", *Signal Integrity Journal,* March 10, 2017
4. ANSYS, Inc. Headquarters, Southpointe, 2600 Ansys Drive, Canonsburg, Pa., 15317, U.S.
5. Keysight PathWave Advanced Design System (ADS) [computer software], (Version 2023, Update 2).
6. Polar Instruments Si9000 [computer software], (Version 22.09.01).
7. IEEE802.3ck COM v3.70, computer software.

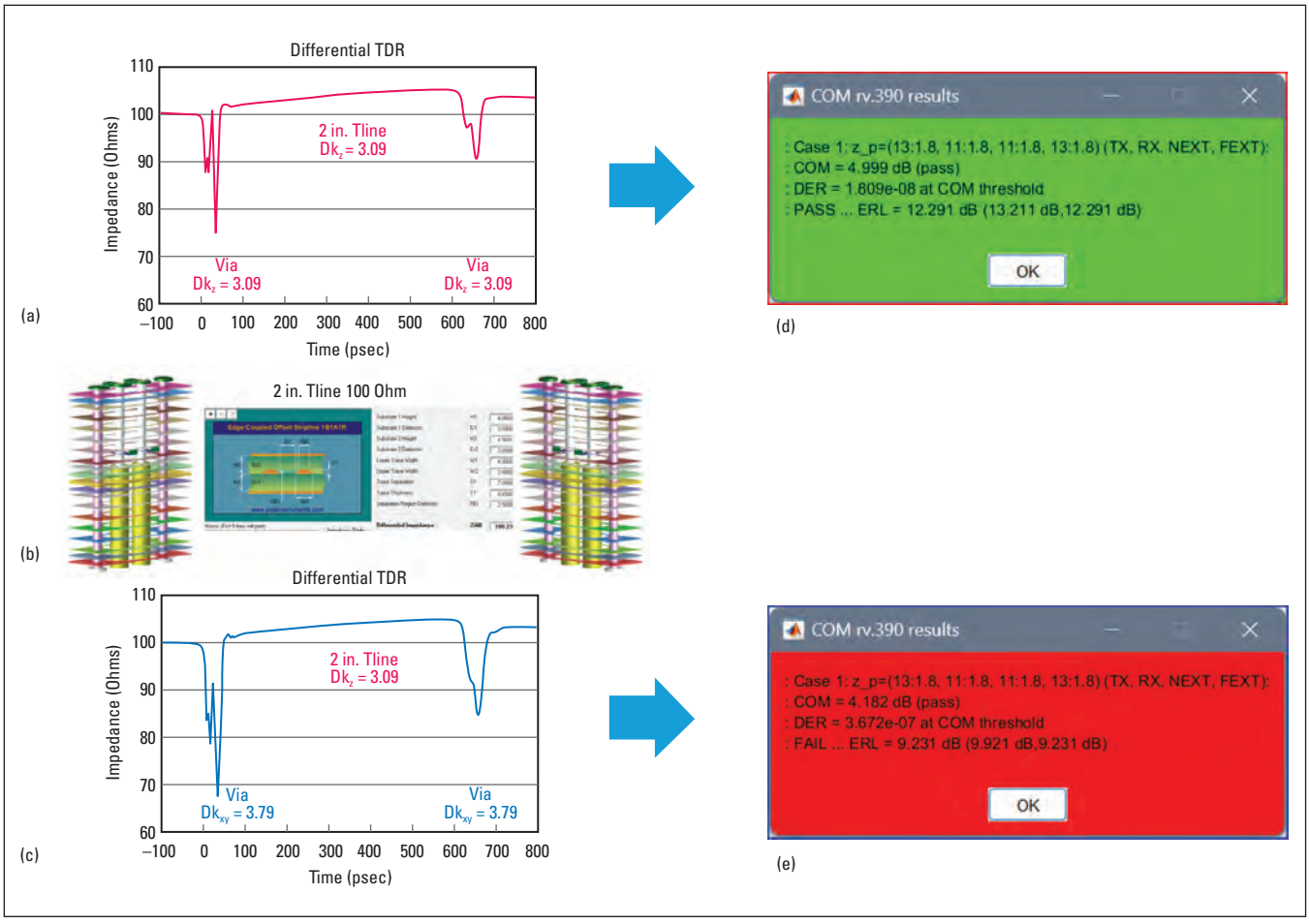

Fig. 6 Simulated TDR and COM results when Dk_z was used for vias and transmission lines compared to when Dk_{xy} was used for via models and Dk_z used for transmission lines. When Dk_z was used for all models COM and ERL passed (d), but when Dk_{xy} was used for the via models, COM passed with reduced margins and ERL failed (e).

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In recent years, the IEEE Electrical Packaging Society (EPS) technical committee for electrical design, modeling, and simulation (TC-EDMS) recognized the need for open-source benchmarks for the simulation tool, verification, and test and measurement solution vendors. The intention is to overcome the obstacles that developers and users of such tools and instruments often encounter and create a growing library of benchmark cases for signal and power integrity challenges.[1,2] As of October 2023, there are four published benchmark cases in the repository. This document describes a proposal for a fifth benchmark.

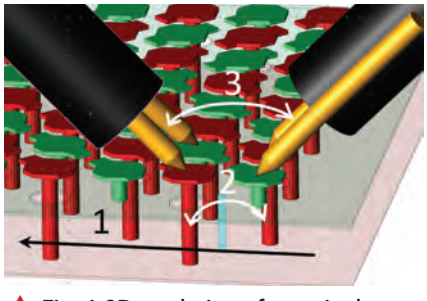


Fig. 1 3D rendering of two single-ended wafer probes touching down on the corner of a large via array, illustrating the three possible areas of investigation: 1) probe-tip coupling, 2) via-loop coupling, and 3) spatial effects.[3]

This benchmark is based on the simulation and measurement challenges and test board features that are described in Koether, et al.[3,4]

Common Test Platform

The overall purpose of this board is to provide the industry with an open-source common test platform that is available to users and can be built by the users if they wish. CAD companies can use the platform to compare simulation tools and setups across different types of simulators from different CAD companies. The platform will allow instrument vendors to refine measurement, calibration, and de-embedding solutions, enabling them to eventually come to a reasonable correlation between simulated and measured values. A common open-source hardware platform would allow various CAD and instrumentation companies to compare their results without sharing confidential details.

The intended use of this benchmark test board is to facilitate the investigation of three areas: to analyze the impact of probe-tip coupling in wafer probe calibrations and measurements; to investigate the impact of via coupling within the device under test; and to better understand the spatial effects associated with large via arrays in low impedance power distribution networks. The associated pieces in a power distribution

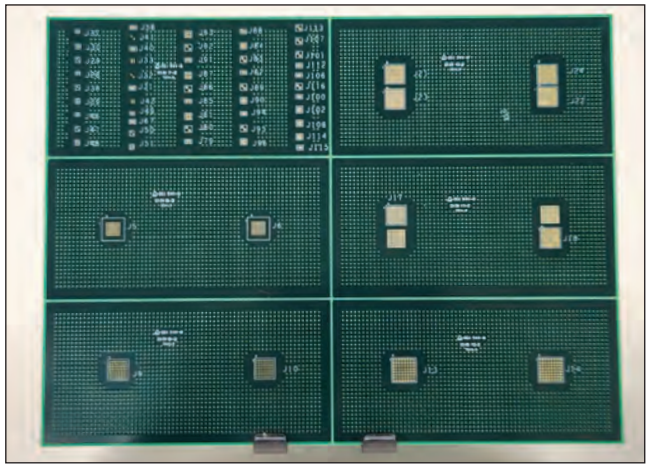


Fig. 2 Front-view photo of the manufactured benchmark board as described in this article.

network (PDN) are illustrated in ***Figure 1***.

This benchmark board is not intended for high-frequency modeling, high-frequency correlation, or high-frequency laminate characterization. This board is designed for wafer probe connections, not for direct coaxial connection.

Description of the Board

The board has six metal layers and can be built with low-cost foil construction lamination and with low-cost laminate materials. The same stackup can also be built with different laminates, not only with the one described here. Note that some of the power-ground laminates, especially the very thin ones, may require a sequential lamination process required by the laminate itself.

The 10 × 7.5 in. board is divided into six identical rectangular areas or sections, as shown in ***Figure 2***. As described in detail later, each rectangular section has full planes within and only within their own boundaries, on all of their four internal core layers. The TOP and BOTTOM layers are pad only.

Stackup

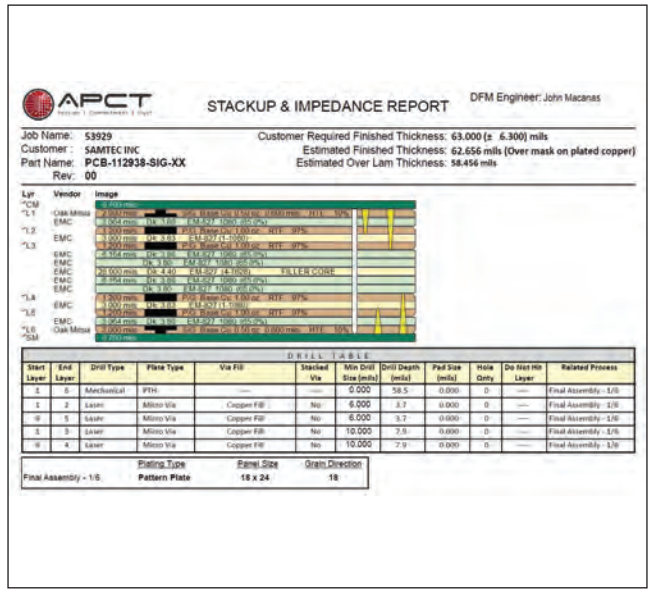
The default board stackup, used for the first build, is shown on a PCB fab vendor drawing in ***Figure 3***. Within practical limits, the same board construction can be built not only with different laminates, but also with different stackup-number targets. Some of the main stackup option considerations are summarized later.

Materials

The first boards were built with the same kind of laminate throughout all of the layers, EMC EM-827, which is considered to be equivalent to Isola 370HR, the popular low-frequency laminate. ***Figure 4*** shows the major mechanical and electrical properties of the laminate.

Construction, Stackup, and Material Options

As will be shown later, there are plated through hole arrays in two of the sections and blind via arrays in three of the sections. One section has various combinations of reference vias, both blind vias and through vias.



APCT STACKUP & IMPEDANCE REPORT

DFM Engineer: John Macanas

Job Name: 53929
Customer: SAMTEC INC
Part Name: PCB-112938-SIG-XX
Rev: 00

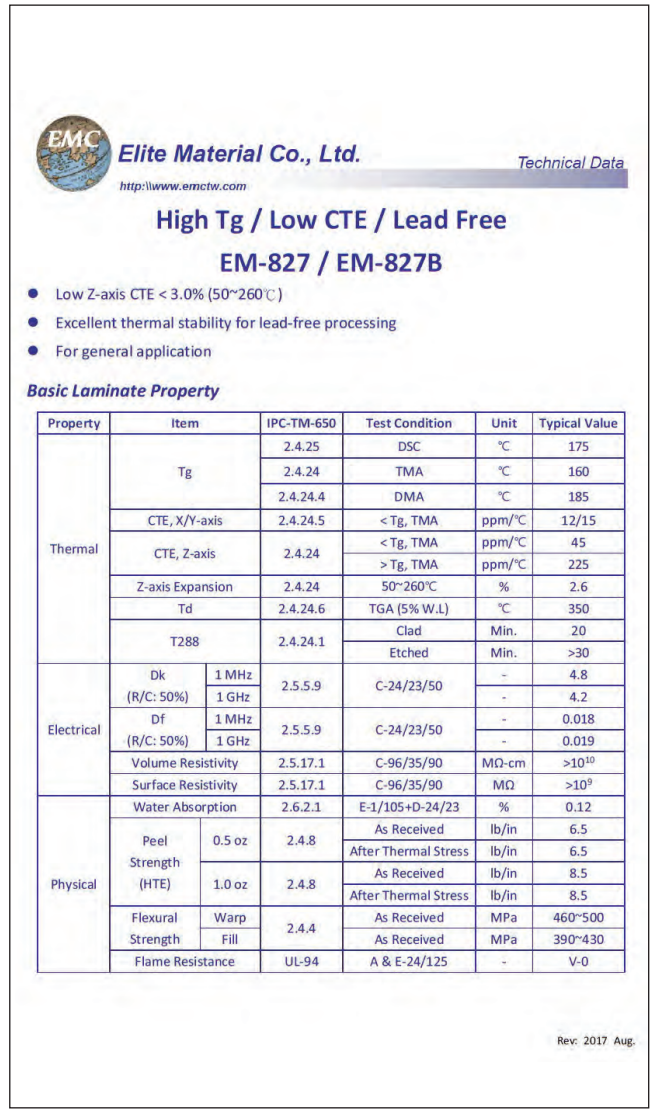
Customer Required Finished Thickness: 63.000 (± 6.300) mils
Estimated Finished Thickness: 62.656 mils (Over mask on plated copper)
Estimated Over Lam Thickness: 58.456 mils

DRILL TABLE

Start Layer	End Layer	Drill Type	Plate Type	Via Fill	Stacked Via	Min Drill Size (mils)	Drill Depth (mils)	Pad Size (mils)	Hole Qnty	Do Not Hit Layer	Related Process
1	6	Mechanical	PTH	—	—	0.000	58.5	0.000	0	—	Final Assembly - 1/6
1	2	Laser	Micro Via	Copper Fill	No	6.000	3.7	0.000	0	—	Final Assembly - 1/6
6	5	Laser	Micro Via	Copper Fill	No	6.000	3.7	0.000	0	—	Final Assembly - 1/6
3	5	Laser	Micro Via	Copper Fill	No	10.000	7.9	0.000	0	—	Final Assembly - 1/6
6	4	Laser	Micro Via	Copper Fill	No	10.000	7.9	0.000	0	—	Final Assembly - 1/6

	Plating Type	Panel Size	Grain Direction
Final Assembly - 1/6	Pattern Plate	18 x 24	18

Fig. 3 Typical stackup and drill definitions of the board. The nominal dimensions and materials are shown for the first build.



Elite Material Co., Ltd.
http:\\www.emctw.com
Technical Data

High Tg / Low CTE / Lead Free
EM-827 / EM-827B

- Low Z-axis CTE < 3.0% (50~260℃)
- Excellent thermal stability for lead-free processing
- For general application

Basic Laminate Property

Property	Item		IPC-TM-650	Test Condition	Unit	Typical Value
Thermal	Tg		2.4.25	DSC	℃	175
			2.4.24	TMA	℃	160
			2.4.24.4	DMA	℃	185
	CTE, X/Y-axis		2.4.24.5	< Tg, TMA	ppm/℃	12/15
	CTE, Z-axis		2.4.24	< Tg, TMA	ppm/℃	45
				> Tg, TMA	ppm/℃	225
	Z-axis Expansion		2.4.24	50~260℃	%	2.6
	Td		2.4.24.6	TGA (5% W.L)	℃	350
	T288		2.4.24.1	Clad	Min.	20
				Etched	Min.	>30
Electrical	Dk (R/C: 50%)	1 MHz	2.5.5.9	C-24/23/50	-	4.8
		1 GHz			-	4.2
	Df (R/C: 50%)	1 MHz	2.5.5.9	C-24/23/50	-	0.018
		1 GHz			-	0.019
	Volume Resistivity		2.5.17.1	C-96/35/90	MΩ-cm	$>10^{10}$
	Surface Resistivity		2.5.17.1	C-96/35/90	MΩ	$>10^{9}$
Physical	Water Absorption		2.6.2.1	E-1/105+D-24/23	%	0.12
	Peel Strength (HTE)	0.5 oz	2.4.8	As Received	lb/in	6.5
				After Thermal Stress	lb/in	6.5
		1.0 oz	2.4.8	As Received	lb/in	8.5
				After Thermal Stress	lb/in	8.5
	Flexural Strength	Warp	2.4.4	As Received	MPa	460~500
		Fill		As Received	MPa	390~430
	Flame Resistance		UL-94	A & E-24/125	-	V-0

Rev: 2017 Aug.

Fig. 4 EM-827 material properties.

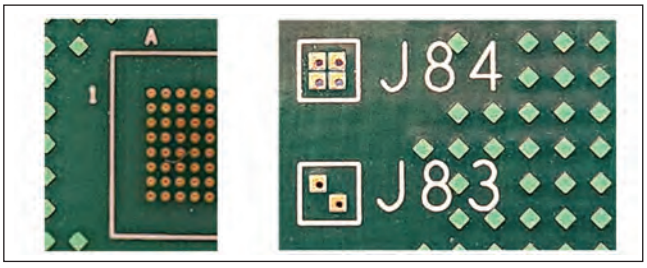


Fig. 5 Illustration of gold surface finish, green solder mask, silk screen for via arrays and reference patterns, and thieving pattern on the outer layers of the board.

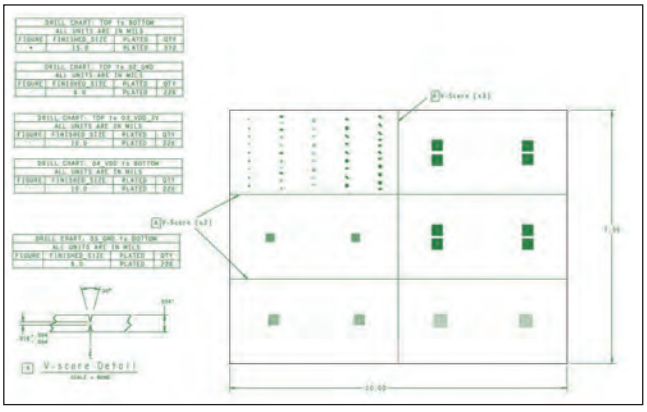


Fig. 6 Fab drawing detail showing the outer dimensions (10 x 7.5 in.).

There are no buried vias in the board and no sequential lamination is required, unless a stackup variant is used with very different core laminates, either much thinner or much thicker. In the former, the laminate itself may require sequential processing; in the latter, reaching layer 3 from the top or layer 4 from the bottom may not work with blind vias.

The thin outer prepreg allows us to keep the low-cost foil construction and use laser-drilled blind vias as long as the smallest-pitch via array can accommodate the L1-L3 and L6-L4 skip vias, which normally would be limited by the maximum allowed aspect ratio.

The current construction allows stackup variants with thinner L2-L3 and L4-L5 cores and/or heavier copper on those cores. In addition to different copper thicknesses, different copper types, and/or different roughness values can also be used, though roughness is usually considered of secondary importance in power distribution networks. For easy comparison across different builds, the overall board thickness can be held constant while using different laminate thickness and copper weight options by adjusting the thickness of the middle prepreg accordingly. Alternately, the total board thickness can also be made different on purpose if the user wants to study and correlate via structures reaching to various depths.

Board Finish and Silkscreen

Though this board does not assume any soldered assembly, and in general it may have very little direct influence on the power distribution performance of the board, passivation of exposed copper is still recommended. The board was built with a flash gold surface finish. The exposed dielectric on the board surface is covered by the customary green solder mask; again, since this board is primarily for lower-frequency PDN tests, the solder mask has very little influence on the performance in that frequency range. To help locate various structures during measurements, the board has silkscreen on the top and bottom. In the board file, each group of vias has a reference designator, and the vias have pin IDs assigned.

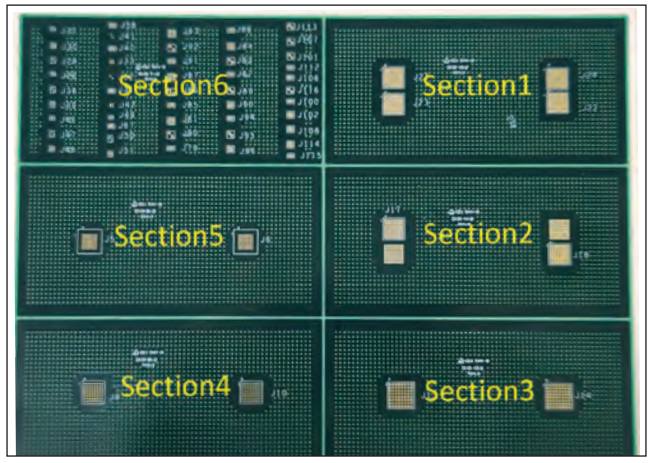


Fig. 7 Top board view displaying the numbering of the six sections.

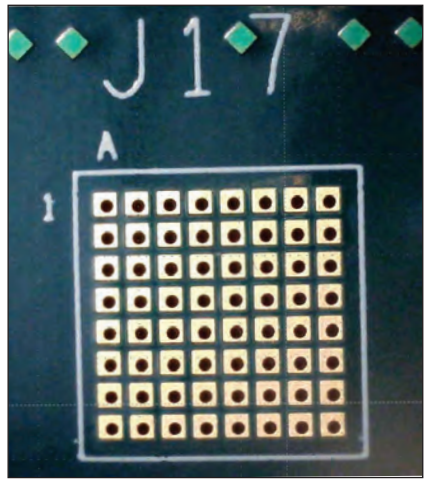


Fig. 8 8 x 8 via array on Sections 1 through 5.

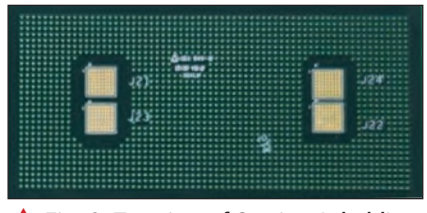


Fig. 9 Top view of Section 1, holding four 1 mm plated through hole arrays.

Finally, the surface has a thieving pattern that covers all unused areas. The thieving pattern for this board is small diamond shapes, but as long as the size of each copper feature is much less than the wavelength, the size and shape will not matter. ***Figure 5*** illustrates these features.

Layout

The fab drawing image in ***Figure 6*** shows that within the 10 × 7.5 in. envelope, there are six sections with identical plane sizes on L2, L3, L4, and L5. The planes in each section are 4.925 × 2.425 in. in size. The six sections, numbered clockwise, are referred to as Sections 1 through 6, as shown in ***Figure 7***.

Sections 1 through 5 have 8 × 8 via arrays with different via pitches, different connections, and different technologies. Section 6 is a reference section, with two or four vias using the plane connections and via technology that we have in Sections 1 through 5. ***Figure 8*** shows the top view of a 1 mm plated through hole array. Pin A1 is connected to GND in all arrays; from there, the pins follow a checker-board pattern and alternate between power and ground.

Overview of Sections

While each section serves a useful purpose, this document focuses on two sections, Section 2 and its corresponding reference features in Section 6.

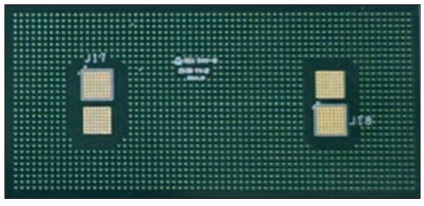


Fig. 10 Top view of Section 2, holding four 1 mm plated through hole arrays.

Section 1

In Section 1, all four via arrays, with reference designators J21, J22, J23, and J24, are connected to both plane cavities, thus allowing us to look at vertical attenuation patterns in PDNs (see ***Figure 9***). Note that in this section, all four via arrays are interconnected together through the planes.

Fig. 11 Via and padstack definition of the 1 mm plated through hole arrays.

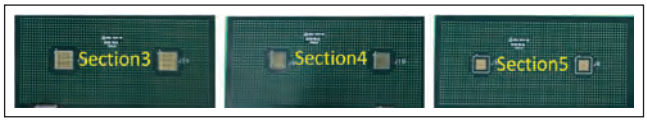


Fig. 12 Top view of Sections 3, 4, and 5.

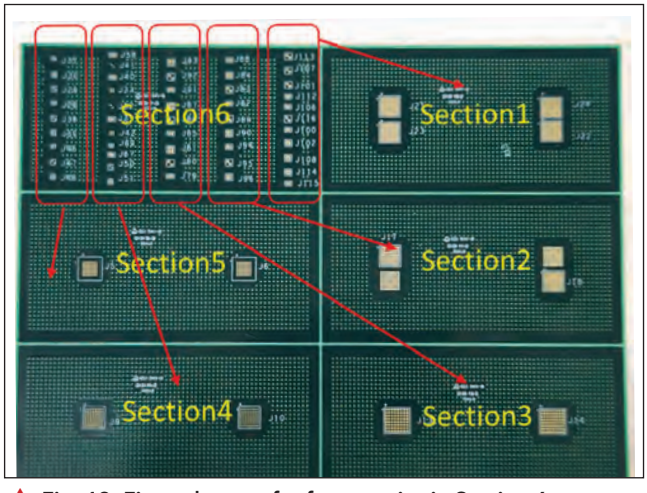


Fig. 13 Five columns of reference vias in Section 6.

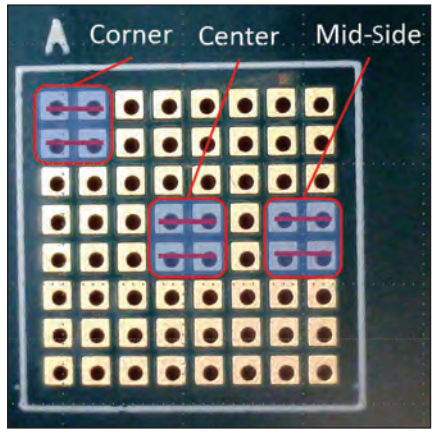


Fig. 14 Connectivity in the reference via groups referring to Section 2.

Section 2

As shown in ***Figure 10***, Section 2 has four 8 x 8 via arrays: J17, J18, J19, and J20. J17 and J18 connect to the L2-L3 plane cavity, whereas J19 and J20 connect to the L4-L5 plane cavity. The via pitch is 1 mm (approximately 40 mil), same as in Section 1; the padstack for the through via is captured in ***Figure 11***. Note that because all four arrays use through holes and all four arrays are accessible from both the top and bottom side, the two sets of two via arrays are not connected together.

Sections 3 Through 5

These three sections use blind vias. Each section has four via arrays — two on the top, connecting to L2 and L3, and two on the bottom, connecting to L4 and L5. Section 3 uses 1.27 mm (50 mil) via pitch, whereas the via pitch in Sections 4 and 5 is 1 mm and 0.8 mm, respectively; see ***Figure 12***.

Because the blind vias do not go through the board vertically, we can place the via arrays at the same X-Y location. Note that as long as we keep the stackup symmetric and balanced, the two via arrays on the top and

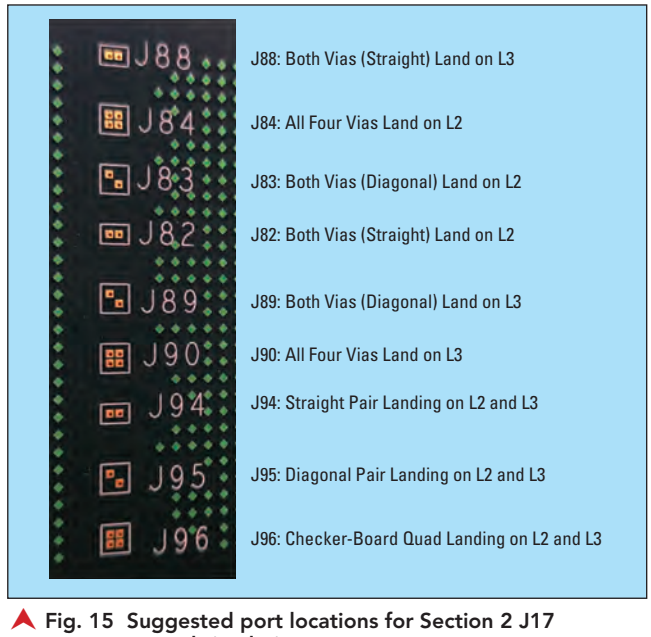


Fig. 15 Suggested port locations for Section 2 J17 measurements and simulations.

Fig. 16 Suggested port orientation for measurements and simulations in Section 6 J84.

on the bottom should behave identically. The reason for the duplication is that it allows us to do redundant measurements.

Section 6, Reference

Section 6 has the various via types, sizes, and pitches that are used on Sections 1 through 5 in groups of two and four vias, making it simpler and easier to measure and correlate. Also, most of the reference vias connect intentionally to the same planes, which allows us to analyze shorter and longer via loops without the added complexity of a plane cavity. As shown in ***Figure 13***, the reference vias in Section 6 are arranged in five columns, corresponding to the five sections with different via arrays. ***Figure 14*** shows the connectivity of each of the nine reference via groups.

Focus Area

Section 2 offers the opportunity to probe via arrays that are connected to one plane cavity only. Moreover, the through vias allow us to probe in various configurations. To name a few obvious choices: we can probe at the selected via pair from top to bottom, and at adjacent or more distant neighbor via pairs from the same side, either top or bottom. The spatial effect can be looked at by probing the structure at different locations; for instance, at the corner, center, and at the mid-point of a side. The suggested locations in ***Figure 15*** also provide the possibility to get transfer parameters between more distant locations.

If we probe power-ground vias in the via arrays with nothing attached to the board, we actually probe an open-terminated plane cavity that represents capacitive reactance at low frequencies. At high frequencies, where the modal resonances of the planes develop, we could also collect information about the dielectric properties. If we limit ourselves to frequencies below the modal resonances, we need a shorted structure so that we can assess the resistance and inductance of the structure. We can solder a shorting plane over the second via array on the planes, in this case, J18, but it may require a professional BGA soldering station to do so properly and repeatedly. Alternatively, we can easily create removable shorts by clamping a carefully flattened copper sheet, cut to the proper size, over the entire via array of J18. To make sure that the connection is repeatable, we can apply silver paste on the shorting copper sheet.

To complement the data that we can collect on the via arrays, the reference via groups offer further correlation opportunities, as several of them create a directly shorted conductive path without the need to go through the plane cavity and the second via array to create a closed loop. For instance, we can measure the via group in J84 in different configurations, preferably with the same port orientation and port assignment that we use for the three locations at J17 (see ***Figure 16***). The four vias in J84 can be considered as a cutout from J17 at the three selected locations, with the only difference being that all four vias are connected to L2, shorting them together. Even though we have only four vias in the group, this structure, just like several of the other reference via groups, offers a large number of possible permutations to simulate and/or to measure. Note that via group J90 similarly connects all four vias to the same plane, but it is L3 instead of L2.

Summary

Eventually, when the design becomes open-source, the goal is to make available the following material:

- Native Allegro board file, Gerber files, ODB++ files, and IPC2581 files
- Schematics file in native Cadence format, as well as in industry standard IPC-356 and PDF formats
- Material and stackup definitions of the manufactured boards
- Sample measurement data on Section 2 and Section 6
- Sample simulation data on Section 2 and Section 6.

The documentation will enable users to fabricate the benchmark boards themselves, either in its default construction or in any variant of it. The default benchmark board may also become available for purchase.

In addition to the documentation, script(s) to analyze, compare, and post-process measured and simulated data may also become available in the future.

Acknowledgements

The authors wish to thank Heidi Barnes and every member of the IEEE TC-EDMS Packaging Benchmarks Committee as well as Patrick Davis and Jonathon Hendren of Cadence; Richard Zai of PacketMicro; and Jean-Remy Bonnefoy, Steve Duzan, and Julia Van Burger of Samtec for their help and assistance with this project.

REFERENCES

1. IEEE EPS TC-EDMS Packaging Benchmark Suite, 2021. [Online]. Available: https://packaging-benchmarks.org.
2. H. Barnes, et al., "The IEEE EPS Packaging Benchmark Suite," *IEEE 2022*.
3. E. Koether, et al., "3D Connection Artifacts in PDN Measurements," *DesignCon 2023*.
4. E. Koether, et al, "Impact of Finite Interconnect Impedance including Spatial and Domain Comparison of PDN Characterization," to be published at DesignCon 2024.

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Assessing the Accuracy of EM Simulation Tools

Aakriti Srivastava
Micron, Boise, Idaho

Eric Bogatin, Melinda Piket-May, Mohammed Hadi, and Aditya Rao
University of Colorado, Boulder, Colo.

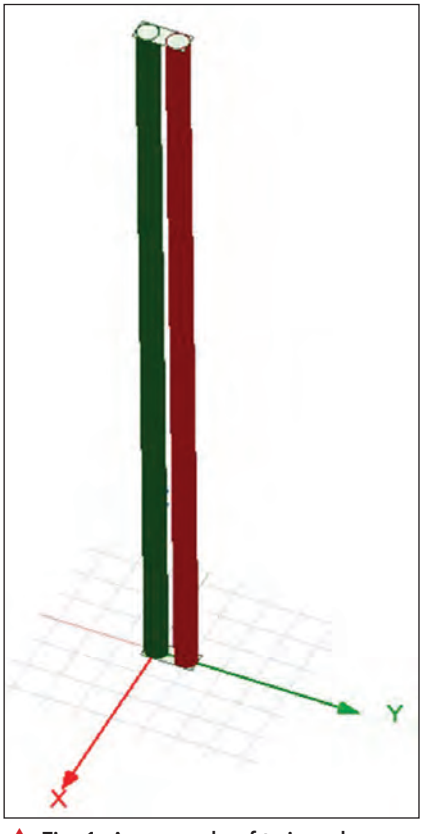

Fig. 1 An example of twin rod structure: two round cylinders with a fixed pitch.

Electromagnetic simulation tools will almost always give a result for any problem after pressing the run button. But is the result accurate? A methodology is introduced to establish the best practices for using the Ansys 2D Extractor and HFSS tools that include recommendations for the setup conditions, balancing accuracy, and computation time. With this methodology, an error in the absolute accuracy when solving for some electrical features can be achieved to better than 0.3%. This methodology can be extended to other more complex structures and applied to other field solver tools.

Methodology

When using a field solver tool for the first time, it is a best practice to simulate something for which you know the answer.[1,2,3] This way, you are able to apply Bogatin's Rule #9: anticipate before you simulate.[4]

One interconnect figure of merit that is important to calculate with a field solver is the characteristic impedance of a uniform transmission line. The twin round rod is a structure that can be analytically solved exactly. The methodology presented here is for setting up a field solver tool and evaluating the characteristic impedance of a twin rod pair. An example of the typical structure simulated is shown in ***Figure 1***.

The characteristic impedance of a twin rod has an exact analytical expression given by

$$Z_0 = (376.73/pi\sqrt{Dk})\cosh^{-1}(s/2r) \quad (1)$$

where s is the pitch (center to center spacing), r is radius of each cylinder, and Dk is the relative permittivity of the medium completely surrounding it.

This analytically calculated characteristic impedance is a reference that can be used to verify the accuracy of any numerical simulation tool. In this article, this methodology is applied to exploring the Ansys 2D Extractor and HFSS full wave solver. This analysis applies equally well to the full version and the free student version.[5]

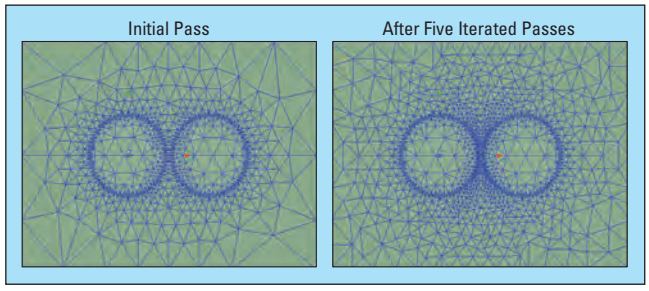

Fig. 2 Example of the mesh generated initially and after five passes.

Setting Up the 2D Extractor

Once the geometry is created in the 2D Extractor and the signal and ground conductors are defined, the only parameter to adjust is the criterion for convergence. Every field solver tool will create a mesh in which Maxwell's equations are approximated and solved. The accuracy of any tool is fundamentally related to the density of the mesh and how well the equations are approximated in each mesh element.

Typically, the more mesh elements there are, the longer the computation time, but the higher the accuracy. The Ansys 2D Extractor uses an adaptive mesh generator which optimizes the mesh so that each time it is refined, more mesh elements are created where there is the highest field gradient. This optimizes the number of mesh elements for accuracy and compute time.

For example, ***Figure 2*** shows the mesh generated for the initial pass and for the fifth pass. The new mesh elements are created where the field gradient is highest. How many passes are enough?

The number of passes to refine the mesh can be set manually or automatically based on a convergence criterion labeled as delta energy. This term is the percentage change in total energy from the previous adaptive pass to the current pass, relative to the total energy calculated in the previous pass. The total energy is the integral of the energy in the electric field throughout the volume of the problem. As the mesh is refined, the total energy in the electric field will converge to a final value, and the change in each iteration will be smaller.

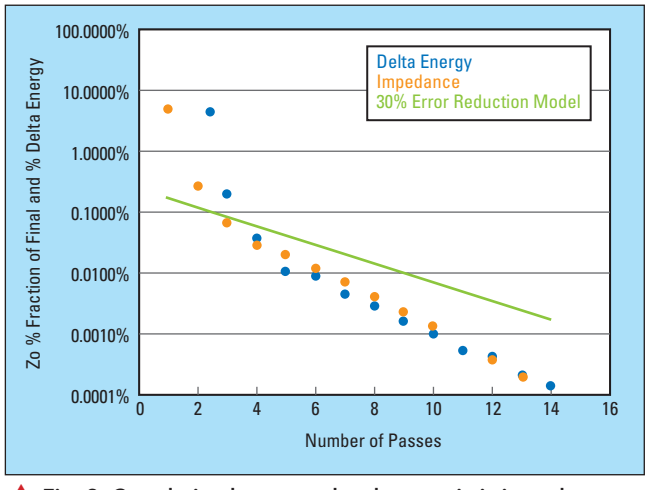

Fig. 3 Correlation between the characteristic impedance and delta energy convergence and a simple model of the error reduction reducing by 30% per pass.

While this is a useful metric of how close to a final answer each iteration might be, it is not clear how this relates to how close to a final value the characteristic impedance calculation might be. To establish the correlation between delta energy change and the final value of the characteristic impedance, a simple numerical experiment was performed.

A twin rod structure was created in the Ansys 2D Extractor tool with air as the surrounding medium. The condition for mesh refinement on each pass was set as a maximum of 30% refinement, the default condition. Passes were iterated manually and after each mesh refinement pass, the characteristic impedance and the delta energy change were recorded. ***Figure 3*** shows the value of the delta energy percent change and the percent difference in calculated characteristic impedance to the final value after pass 25. This is compared with a simple model assuming a 30% reduction in the change per pass.

This comparison illustrates that the delta energy percent change term in each pass closely matches the characteristic impedance convergence to the final value. This establishes confidence that the delta energy convergence value is a good surrogate for the convergence of the final value of other electrical metrics. It also suggests that the improvement in accuracy with each pass increases faster than just the maximum number of mesh elements.

To achieve a calculated value of characteristic impedance that is within 0.1% of the final value, the delta energy convergence should be set to a value of 0.05%.

Translating the Real Problem into the Tool Environment

The next step is deciding how to translate some of the features of the real structure into the 2D Extractor environment. A round structure is described in rectilinear geometry as a polygon with a finite number of facets. How many facets around the circumference are enough?

As a simple numerical experiment, the number of facets of each rod was increased and the characteristic impedance was calculated using the convergence criterion of 0.001% delta energy for each calculation. The difference in calculated characteristic impedance for each number of facets with the final value for more than

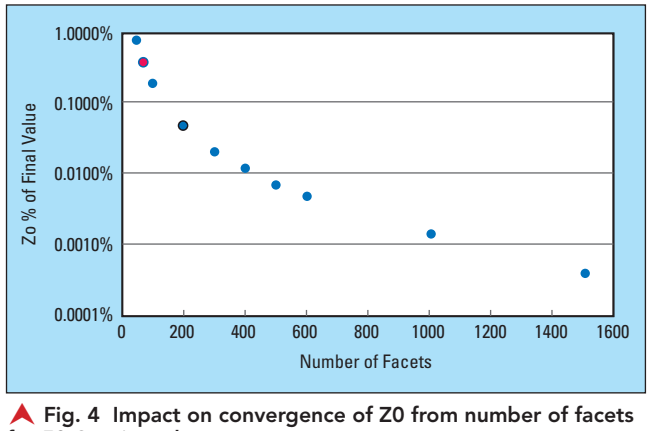

Fig. 4 Impact on convergence of Z0 from number of facets for 50 Ω twin rods.

1500 facets was simulated as the number of facets increased. ***Figure 4*** shows the reduction in the difference between the characteristic impedance and the final value. It is interesting to note that while the Ansys manual does not state the default number of facets used, it can easily be reverse engineered. The characteristic impedance value for the case of 70 facets matched the simulated impedance for the default setting. For a value within 0.1% of the final value, a total of 200 or more facets should be used.

Absolute Accuracy of the 2D Extractor

Once the condition for convergence is established as well as the recommended number of facets, the next question is: what is the absolute accuracy of the 2D Extractor tool?

Every simulation is always a balance between compute time and accuracy. In principle, if the numerical solution to Maxwell's equations is implemented correctly, an arbitrary accuracy can be achieved with an arbitrarily fine mesh. We set a starting goal of an absolute accuracy of better than 0.1% error. This requires setting the convergence in the delta energy to 0.05% and the number of facets to 200.

The 2D Extractor uses the background as the extent of the space in which the fields are calculated. This is not a term that can be adjusted, and it is not clear from any documentation on the size of the region. To view the mesh or any calculated field quantities, a boundary region must be created. When this region is filled with air, there does not seem to be any impact on a calculated electrical parameter from the extent of this region.

The analytically calculated impedance of the twin rod structure was 50.000 Ω, while the numerically calculated characteristic impedance was 50.009 Ω. They agree to within 0.02%. This is a direct confirmation of the absolute accuracy of the 2D Extractor tool.

Summary of Best Practices Using the 2D Extractor

Based on simple numerical experiments, a few general guidelines have been established to achieve an absolute accuracy in calculating the characteristic impedance of twin rods in the 2D Extractor tool:

1. Set the delta energy convergence to be lower than the absolute error required. For an error of 0.1%, set the delta energy convergence to 0.05%.
2. When translating a round structure into a faceted structure, use at least 200 facets for an absolute accuracy better than 0.1%.
3. When modeling a homogeneous infinite extent dielectric, change the Dk of the background to match it. When modeling localized dielectric regions, as a starting place, assume the electric fields extend 10x the pitch between conductors to achieve a value within 0.1% of the infinite extent case.

It is remarkable that the absolute accuracy of a numerical simulation can easily approach better than 0.1% error to an analytically exact case. This enables the use of the 2D Extractor as a reference to calculate the characteristic impedance of any arbitrary structure. This methodology and the results of the 2D Extractor are applied directly to establish the best practices for HFSS, a full wave 3D EM solver.

Setting Up HFSS

HFSS is a general, arbitrary, 3D full wave simulation tool. While it is a workhorse tool for antenna and radiated emissions problems, it is becoming a powerful tool to analyze interconnects for signal integrity applications.

When dealing with interconnects imported from circuit board layout structures, lumped ports are typically used. This is the case when there is a single conductor identified as the return path. Otherwise, when there are multiple return conductors and the interconnect structure begins and ends at a uniform transmission line cross section, a wave port is recommended. Lumped ports and a radiation boundary condition were exclusively used in all the problems presented in this article.

The twin rods problem was used to establish confidence in the results from HFSS. While it is the S-parameters of the structure from the lumped ports which are

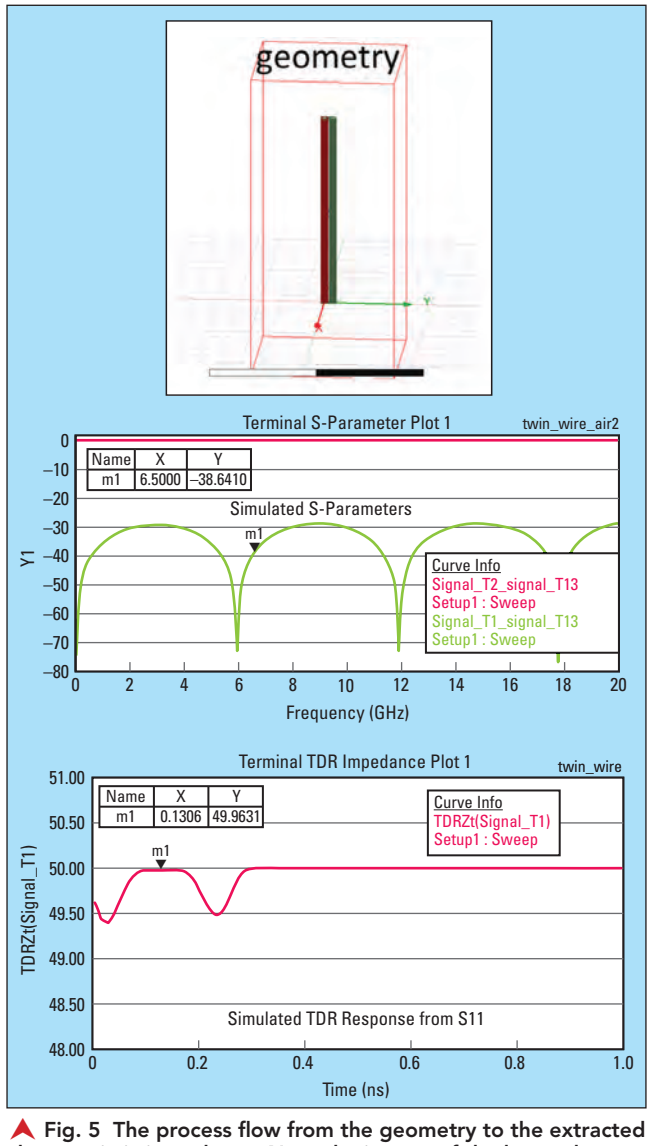

Fig. 5 The process flow from the geometry to the extracted characteristic impedance. Note the impact of the lumped ports in this example is to add a small amount of excess capacitance to the ports.

calculated, this was translated into a characteristic impedance by simulating an electrically long structure and using a TDR simulation of the return loss to extract a value of the characteristic impedance. ***Figure 5*** shows an example of the twin rod structure, the simulated S-parameters, and the simulated TDR from S11.

In setting up the tool, there are a number of parameters to adjust. The methodology of starting with something for which you know the answer and comparing the analytically exact answer with the simulated result was applied to evaluate the best practices for:

- Criteria of delta S for convergence
- The size of the lumped port
- The minimum physical length of the structure to be electrically long and use TDR to get the characteristic impedance.

Convergence Criteria

The convergence criterion in HFSS is based on the largest change in any S-parameter with each iteration. Each iteration refines the mesh in regions in which there are large field gradients. The default maximum increase in mesh elements from pass to pass is 15%. Using the same methodology as with the 2D Extractor, the connection between the convergence in the delta S term and the extracted characteristic impedance can be correlated with the number of iterations. ***Figure 6*** shows this connection.

There is also a good correlation between the delta S condition and the convergence in the characteristic impedance of the twin rod. A convergence in the characteristic impedance to 0.1% of its final value requires a convergence of delta S to better than 0.1%. The correlation between the delta S and the absolute accuracy of the characteristic impedance is structure dependent and not precise. As a starting place, in the case of the twin rod geometry, for convergence in the characteristic impedance to within 0.1% of the final value, the delta S convergence criteria should be at least 50% smaller, or 0.05%. In this example, this required more than 15 passes.

This is based on a very specific geometry. It may vary with other geometries. For example, if the problem involved an electrically short structure, such as a via, in an otherwise large structure, the accuracy of recovering the S-parameters of the via structure may not be indicated with the overall delta S value. This suggests that an important practice is to keep the non-essential structures to a minimum length so they do not dominate the S-parameter convergence.

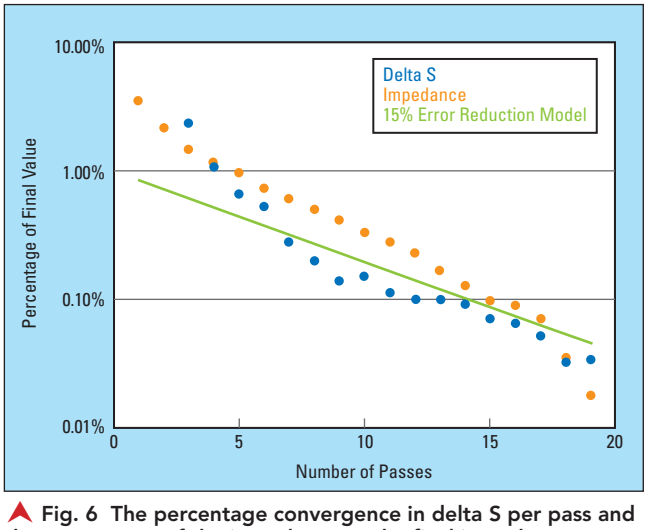

Fig. 6 The percentage convergence in delta S per pass and the percentage of the impedance to the final impedance.

Number of Facets to Approximate Round Structures

When translating a round structure into a faceted structure in HFSS, it was found that 70 facets are required to get a convergence of 0.1% in characteristic impedance to the final value. The results of this analysis are shown in ***Figure 7***. It is also interesting to note that the default condition in HFSS can be reverse engineered as 20 facets. This default condition results in a value that is only within 3% of the final value.

The Size of the Lumped Port

The lumped port, using terminal mode, will connect between the signal and its return path. In the case of

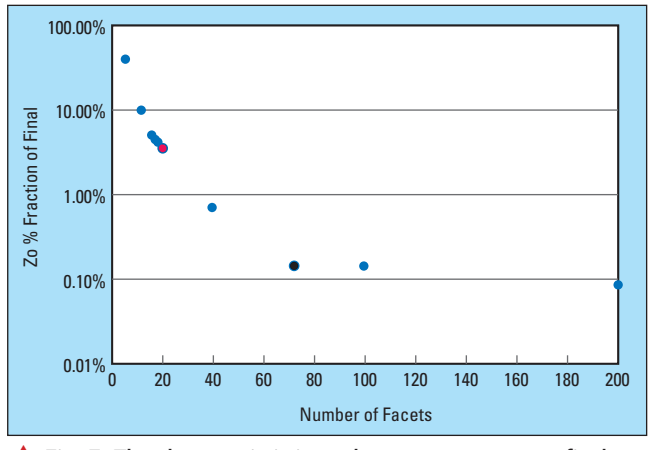

Fig. 7 The characteristic impedance converges to a final value as the number of facets increases.

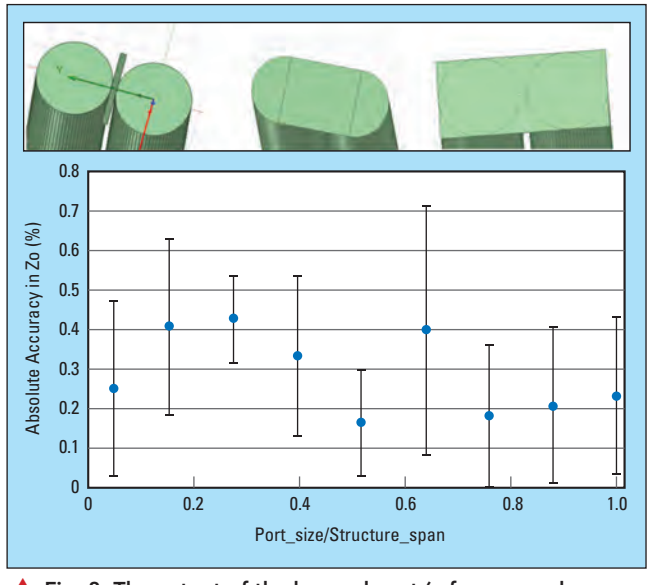

Fig. 8 The extent of the lumped port (a few examples shown in the insert) has no impact on the absolute value of the characteristic impedance to within about 0.5%. The error bars represent the uncertainty in extracting the characteristic impedance from the TDR.

the twin rod, the lumped ports can be as small as the spacing between the twin rods or as large as the extent of the edges of the rods.

Using the conditions of 15 passes and 70 facets, the characteristic impedance was calculated for different lumped port sizes from the minimum dimension just touching the signal and return conductors together and overlapping them. The absolute accuracy of the calculated characteristic impedance did not depend on the lumped port size to within about 0.5% of the absolute accuracy. This result, shown in ***Figure 8***, was limited in accuracy by the 15 passes used.

Electrically Long Structures

In order to use the TDR simulation to extract a value for the characteristic impedance of the twin rod structure, it must be electrically long. This way, the TDR profile will show a flat top or flat bottom from which the characteristic impedance can be interpreted from the constant instantaneous impedance.

This condition is usually based on the common rule of thumb, TD > ½ the rise time.[6] This results in an estimate that the physical length should be larger than about ½ wavelength for the highest frequency used in the simulation. Longer than this physical length, the impedance should not depend on the electrical length.

In these simulations, to see a flat top or flat bottom with better than 0.1% uncertainty, we found that a more robust estimate is TD > rise time. This translates to the electrical length > the wavelength at the highest simulated frequency. This is illustrated in ***Figure 9***.

Summary of Best Practices Using HFSS

Based on a few simple numerical experiments using twin rod structures, some general guidelines have been established to achieve an error in the absolute accuracy in calculating the characteristic impedance in HFSS that is better than 0.3%.

This analysis used lumped ports for the structure under test. This is limited to the case when there is a connection to only one signal and one return conductor. As revealed in the TDR simulations, the lumped ports introduce a discrete excess impedance to the launches. This will ultimately limit the useful bandwidth for very accurate results. However, using TDR to extract the characteristic impedance of an electrically long, uniform transmission line effectively time gates this simulation artifact from the calculation of the characteristic impedance.

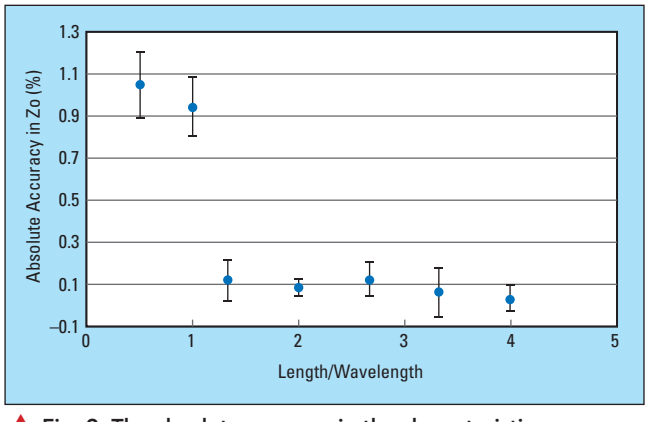

Fig. 9 The absolute accuracy in the characteristic impedance as the electrical length is increased. A robust rule of thumb is that the length should be greater than the wavelength.

This analysis was based on a very special case which may not have a similar geometry to other problems, but it is a starting point to evaluate the process of setting up and using HFSS or other electromagnetic simulation tools.

A best practice when using a new tool is to always start by solving something for which you already know the answer. In this case, a twin rod geometry can be exactly solved analytically and used as a reference. After establishing a methodology of achieving better than 0.1% absolute error in the 2D Extractor tool, any arbitrary structure can be solved in this tool and used as a reference in an HFSS calculation.

There will always be a fundamental trade-off between the complexity of the structure, the absolute accuracy required, and the compute time and resources. The convergence criterion is one term to adjust this balance.

Only one electrical figure of merit, the characteristic impedance of the interconnect, was evaluated in this analysis. But this methodology can be applied to explore the best practices for other criteria, if you start with something for which you know the answer.

The recommended best practice to achieve a level of absolute accuracy in HFSS is as follows:

1. Set the delta S convergence to be 50% lower than the absolute error required. For an error of 0.1%, set the delta S convergence to 0.05%, i.e. the value of delta S in simulation tool is 0.0006. For an error in the absolute value of 2%, use a value of 1%.
2. When translating a round structure into a faceted structure, use at least 70 facets for an absolute accuracy better than 0.1%.
3. The size of the lumped port is not important if it connects the signal and return conductors.
4. The extent of the radiation boundary is not important for calculating a characteristic impedance. It may be important if radiation effects are considered.
5. The minimum physical length of the structure, in order to be electrically long and use TDR to get the characteristic impedance, should be longer than the wavelength of the highest simulated frequency.
6. Be aware that the lumped port does add a small excess impedance to the launches.

REFERENCES

1. J. C. Rautio, "An Ultra-high Precision Benchmark for Validation of Planar Electromagnetic Analyses," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 42, No. 11, Nov. 1994, pp. 2046–2050, doi: 10.1109/22.330117.
2. J. C. Rautio, "Experimental Validation of Microwave Software," *ARFTG Conference Digest*, 1990, pp. 58–68, doi: 10.1109/ARFTG.1990.323981.
3. K. Z. Aghabarati and L. E. Rickard Peterson, "Overview of the Iterative Solver in HFSS for Analysing Frequency Domain Electromagnetic Problems," *International Applied Computational Electromagnetics Society Symposium*, 2019, pp. 1–2.
4. E. Bogatin, "*Signal and Power Integrity-Simplified*," Prentice Hall, 2009.
5. Ansys for Students, https://www.ansys.com/academic/students.
6. E. Bogatin, "*Bogatin's Practical Guide to Transmission Line Design and Characterization for Signal Integrity Applications*," Artech House, 2019.

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Who Put That Inductor in My Capacitor?

Will McCaffrey, Tyler Huddleston, Benjamin Dannan, and James Kuszewski
Northrop Grumman Mission Systems, Baltimore, Md.

The design and performance of power distribution networks (PDNs) in modern printed circuit board (PCB) assemblies and application-specific integrated circuits (ASICs) are paramount for ensuring a stable and clean voltage to the load.[1] To achieve this, accurate modeling of all elements of the PDN is essential.[2] One often overlooked element is an accurate representation of the capacitors that filter voltage ripple at the load and provide a matched impedance from the source to the load. Capacitors are an integral part of any PDN, yet the models used can be compromised by additional inductance introduced during the measurement process. This added inductance creates an error term in the model that affects the capacitor's impedance's accuracy and impacts the PDN's quality.

This error term comes from failing to properly de-embed the measurement mount when characterizing capacitors. Many vendor-provided capacitor models contain extra inductance from the measurement mount that can result in inaccuracies in the representation of capacitor parameters, such as the resonance frequency, equivalent series resistance (ESR), and equivalent series inductance (ESL).[1] This error term can then lead to errors in the simulation of the PDN, concealing resonant Q-points or causing unnecessary over-design efforts to mitigate inductance that does not exist in the physical PDN.

This further emphasizes the importance of proper calibration, measurement, and de-embedding to ensure that the final capacitor model is free of errors, allowing an accurate representation of the PDN used in simulation.[3] While capacitor models may play a seemingly minor role in the overall system design, the impact of capacitor models can significantly impact the system design and, importantly, design sign-off.

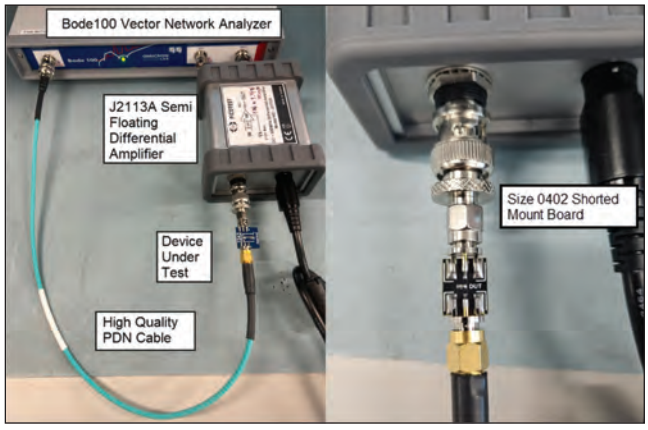


Fig. 1 Image of a shorted mount measurement.

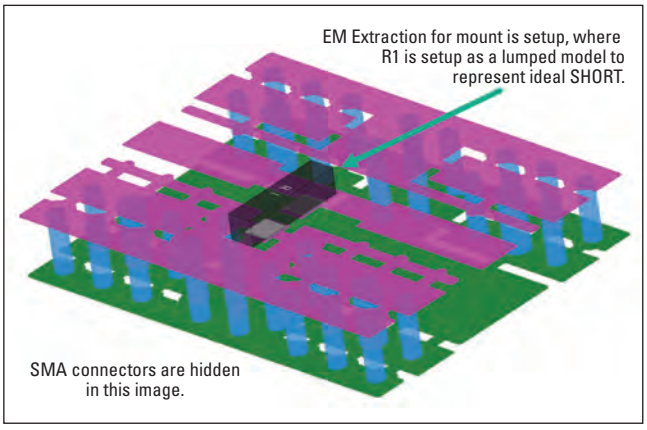


Fig. 2 EM model of short board.

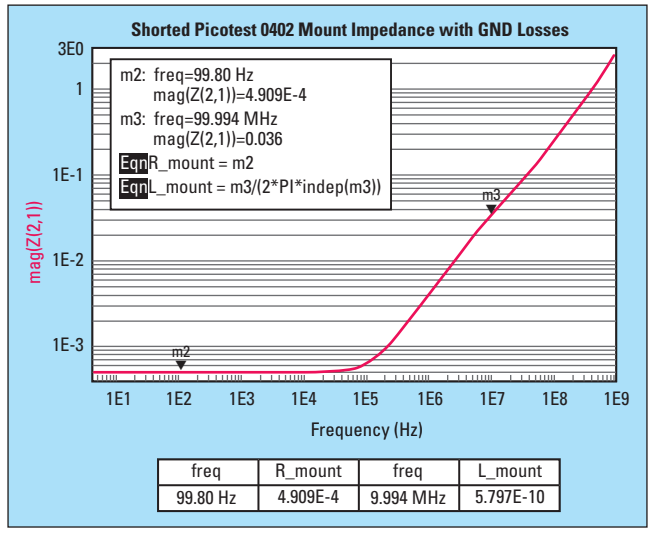
How to Measure Passive Components

Correct and error-free measurements result from proper equipment, calibration techniques, and correlation to known good measurements.[4] ***Figure 1*** shows an image of a frequency response analyzer (FRA), used as a vector network analyzer (VNA), measuring a device under test (DUT). In this case, the DUT is a 0402-capacitor mount board that has been purposely shorted. The measurement of this shorted 0402 mount is then used later to de-embed the mount from measurements of capacitors with 0402 package size. Due to the variety of capacitor sizes, package-specific mount boards are required to hold the capacitors for measurement.

A variety of VNAs, cables, and mounts can be used if they are correctly calibrated and measured. All sources of error in the cables and DUT must be addressed as part of the calibration process. In a 2-port impedance measurement setup, it has been well documented that a ground loop is present and adds error to the measurement result.[5] In Figure 1, the J2113A semi-floating differential amplifier is used in the measurement setup to break the inherent ground loop in the measurement path.[6]

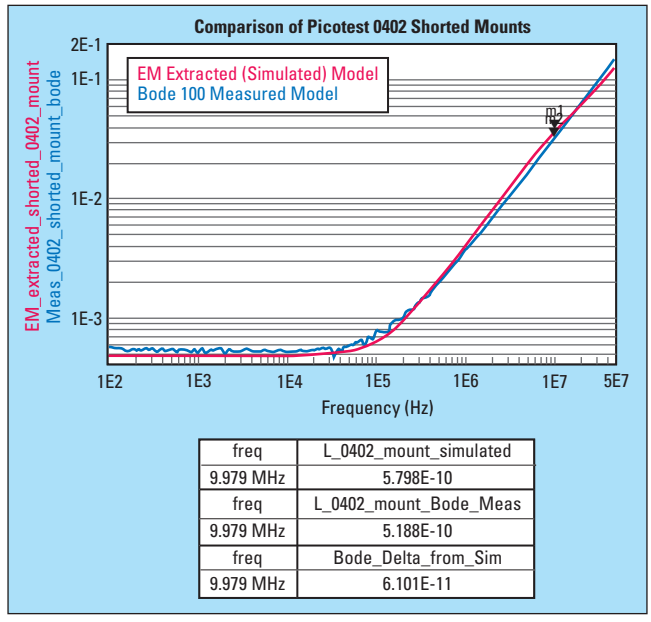
Measurement to Simulation Correlation of a Shorted Mount

An electromagnetic (EM) model of the mount is extracted from the PCB artwork using the finite element method field solver in Keysight PathWave PIPro to build confidence in the measurement. This EM extraction is a Touchstone file in the S-parameter format. Resistive and ground losses are included in the EM model extraction. The EM extraction setup consists of an ideal 0 Ω resistor across the capacitor pads to represent a perfect short. A 3D representation of the model is shown in ***Figure 2***.



freq	R_mount	freq	L_mount
99.80 Hz	4.909E-4	9.994 MHz	5.797E-10

Fig. 3 EM extraction results of shorted 0402 board.



freq	L_0402_mount_simulated
9.979 MHz	5.798E-10
freq	L_0402_mount_Bode_Meas
9.979 MHz	5.188E-10
freq	Bode_Delta_from_Sim
9.979 MHz	6.101E-11

Fig. 4 Comparison of Picotest 0402 shorted mounts, extraction to measurement.

Figure 3 shows the results of the extraction. The shorted 0402 mount board has a low-frequency resistance of 0.49 mΩ up to 10 kHz, as seen with marker m2. At frequencies higher than this, the impact of the mount board's inductance takes over. Marker m3 is placed at 10 MHz, and the measured impedance is 0.036 Ω. Equation (1) gives the inductance of the mount for a given reactance X_L at a frequency f. The shorted 0402 mount inductance is 580 pH.

$$L = \frac{X_L}{2\pi f} \quad (1)$$

Figure 4 shows the results comparing the measurement with the EM extraction of the 0402 shorted

mount. There is a strong correlation between the EM extraction and the measurement of the shorted mount. The EM extracted PCB mount's path inductance is 580 pH, while the measured PCB mount's path inductance is 520 pH. This difference of just 60 pH gives confidence that the simulated model is an accurate way to de-embed the mount.

Why Do We Care So Much About the PCB Mount?

The capacitor mount adds error to the capacitor measurement. The extent of this error varies by the mount used due to dependencies on the arrangement of vias, dielectric material, and copper trace thicknesses. These dependencies warrant that the best method of de-embedding the fixture from a mounted DUT measurement utilizes a characterization of the isolated mount itself. ***Figure 5*** illustrates that the measurement reference points move from the SMA connectors to the capacitor terminals by de-embedding the mount board from the mounted DUT measurement.

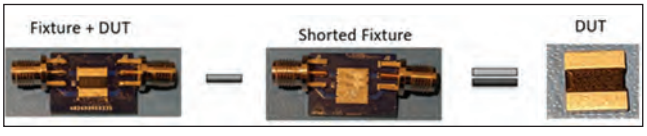
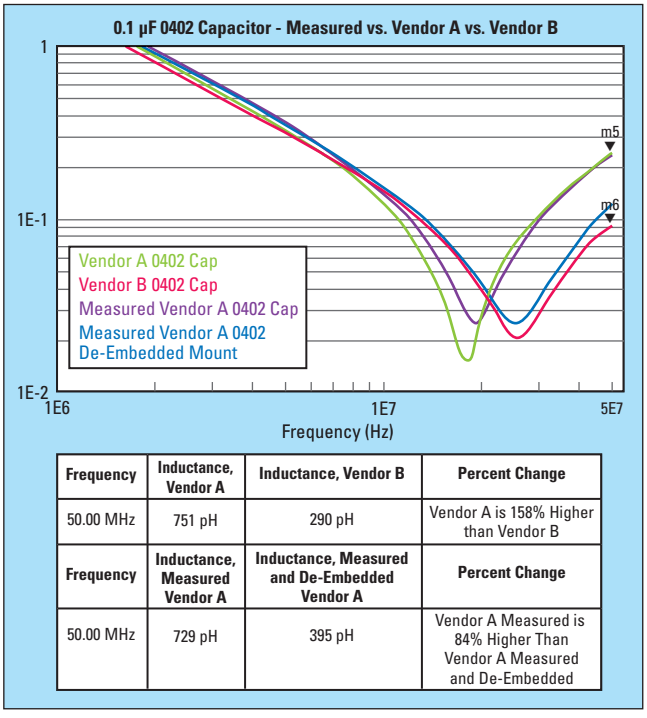


Fig. 5 Graphic of DUT and mount board.[4]



Frequency	Inductance, Vendor A	Inductance, Vendor B	Percent Change
50.00 MHz	751 pH	290 pH	Vendor A is 158% Higher than Vendor B
Frequency	**Inductance, Measured Vendor A**	**Inductance, Measured and De-Embedded Vendor A**	**Percent Change**
50.00 MHz	729 pH	395 pH	Vendor A Measured is 84% Higher Than Vendor A Measured and De-Embedded

Fig. 6 Comparison of a 0.1 µF 0402 vendor models to measurements.

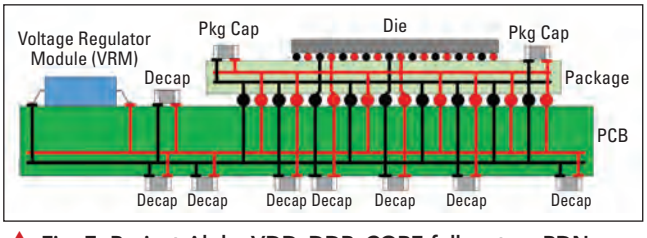


Fig. 7 Project Alpha VDD_DDR_CORE full system PDN layout.

How Does De-embedding Work?

De-embedding takes the overall mounted DUT measurement S-parameters and removes the known parameters of the measurement mount board. In Figure 4, the measurement mount is shorted together with bus wire and measured, and is then compared to the EM extraction of the same measurement mount shorted. The correlation between these two provides confidence that the parameters of the mount board are known and can be removed from the overall measurement S-parameters. What remains are just the S-parameters of the capacitor.[8]

Why does this matter? A power distribution network is robust if its capacitors help provide a matched impedance from source to load. The impedance versus frequency response of the capacitor is a function of the capacitance, its ESL, and ESR. If the PDN simulation uses capacitors with uncorrected error terms in the ESL, the results of the entire simulation are affected.

Currently, passive component models from vendors do not follow a set measurement and de-embed standard. ***Figure 6*** compares a de-embedded and not de-embedded measurement of a 0.1 µF 0402 capacitor against models provided by vendors. Both vendor capacitors had the same voltage and dielectric material. However, notice how the resonance peaks and valleys in the simulation will not line up with measurement due to additional error terms attributed by each capacitor.

The model from Vendor A has an inductance of 751 pH at 50 MHz, shown as the green line, while the model from Vendor B only has an inductance of 290 pH, shown as the red line. Looking further, the Vendor A 0402-capacitor measurement with the mount board included has an inductance of 729 pH, shown as the purple line, which is very similar to the Vendor A model. When that same capacitor is measured and then de-embedded, the capacitor inductance is only 395 pH, shown as the blue line, and is about what is expected.[3] This demonstrates that the Vendor A capacitor likely was not properly de-embedded and has an additional 400 pH of inductance in the model. Vendor A's model has 158% more inductance than Vendor B's model. Vendor A's model also has 84% more inductance than Vendor A's capacitor measured and de-embedded. This lack of de-embedding the measurement mount has been seen on models across many vendors. On a PDN with many capacitors, this error term quickly adds up, causing a significant impact on the accuracy of the simulation.

Complete PDN Simulation with Vendor Capacitor Models and Measurement-Based Capacitor Models

To fully emphasize the impact of the additional ESL in vendor capacitor models, a complete system PDN design was simulated with both vendor and measurement-based capacitor models. This PDN design uses a 0.8 V voltage power domain to supply current to the core rail,

DDR, and PLL circuitry on a custom ASIC, Project Alpha. The complete system PDN model is illustrated in ***Figure 7*** and shown as a block diagram in ***Figure 8***.

The Keysight Advanced Design System (ADS) simulation schematic is shown in ***Figure 9***. This consists of a Sandler State-Space Average Model (SSAM)[10] of the LTM4650-2 Voltage Regulator Module (VRM); the PCB PDN; the substrate PDN (including a remote sense point on the substrate);

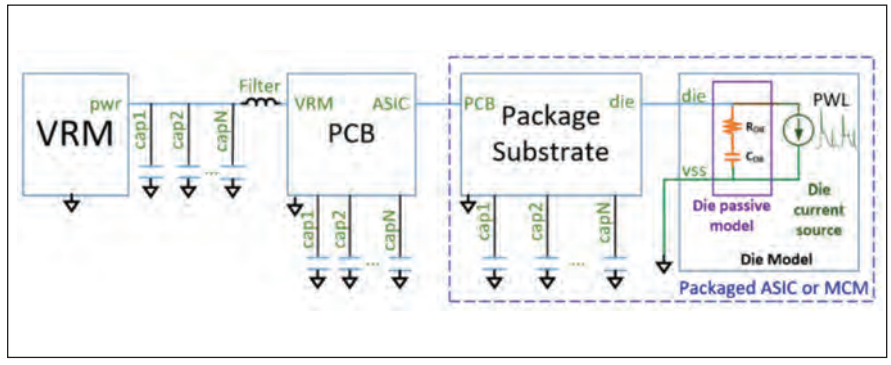


Fig. 8 Project Alpha VDD_DDR_CORE full system PDN simulation block diagram.

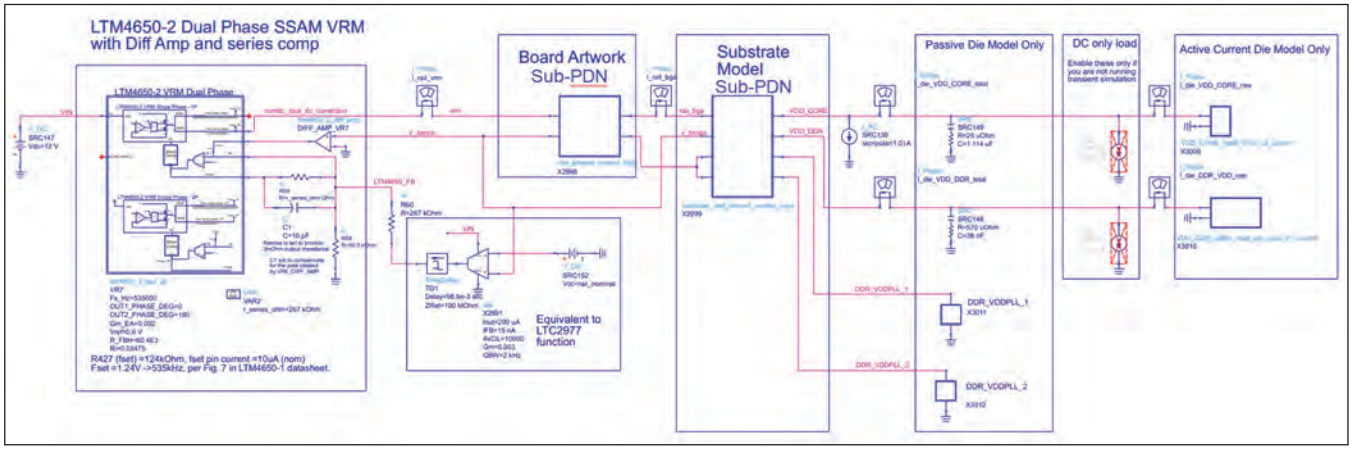


Fig. 9 Project Alpha full system PDN simulation model with VDD_CORE and VDD_DDR die models.

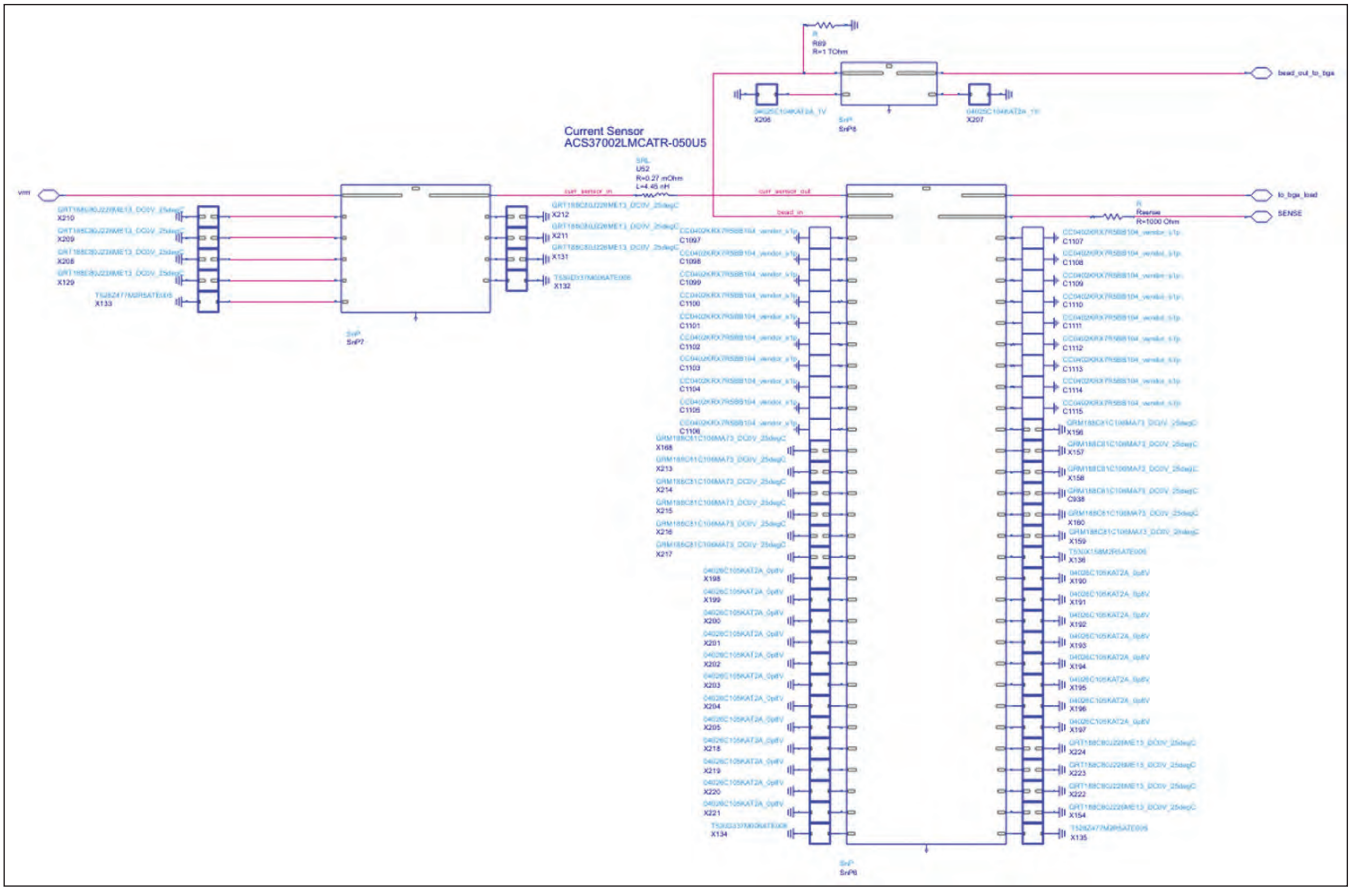


Fig. 10 Sub-PDN model containing extracted PCB artwork with vendor capacitor models.

a power manager LTC2977; and die models for the core rail, DDR, and PLL circuitry. The PCB and substrate models are EM extractions of the artwork and include ports for attaching the decoupling capacitor models, as shown in the sub-PDN models of ***Figures 10*** and ***11***. The capacitor models are either vendor models or lumped element broadband SPICE models fitted to the de-embedded S-parameter measurements of the actual capacitors to ensure simulation coverage outside the frequencies in the measured S-parameter model. These core and DDR die models contain piece-wise linear waveforms representing time domain current demands on the PDN. The passive and active current die models are SPICE extractions from the die circuitry designs, extracted using Cadence Voltus. This system model allows both frequency domain and time domain analysis.

The simulation results of Figure 9 (using the sub-PDNs shown in Figures 10 and 11) were compared to the same simulation except replacing the vendor capacitor models with measurement-based capacitor models. The comparison results for the DDR_VDD rail are shown in ***Figure 12*** and the results for the CORE VDD rail are shown in ***Figure 13***.

Due to the additional ESL included in the vendor capacitor models, the PDN yields a false additional impedance peak at 21 MHz, as shown by marker v2 in Figure 12 and marker v4 in Figure 13. This peak is 3x greater (about 24 mΩ higher) than the nearest impedance peak at marker m2 in Figure 12 and marker m4 in Figure 13, and exceeds the target impedance. Typically, a PDN designer would try to correct the impedance resonance by adding more capacitance, leading to over-design. Since this impedance peak is not real, by adding more capacitance, designers may inadvertently create sharp anti-resonances, making the PDN unstable.[11]

Also observed in Figures 12 and 13 is a significant impedance difference at the lower frequencies, as seen at markers vl1 in Figure 12 and vl2 in Figure 13. At 250 kHz, vendor models attribute 296 pH more inductance on the DDR VDD rail and 288 pH more on the CORE VDD rail.

As discussed in Dannan et al.[9], initial power integrity analysis happens in the frequency domain. However, design sign-off must occur in the time domain. ***Figures 14*** and ***15*** demonstrate the time domain voltage ripple results of the Figure 9 simulation, as observed at the die bumps using vendor capacitor models (see Figure 14) and instead using measurement-based capacitor models (see Figure 15). These results are summarized in ***Table 1***, which shows a 5.5 mVpp, or 11.77%, greater voltage ripple with vendor capacitor models. This is caused by the false additional PDN impedance peak, which, if trusted, could be the difference between passing or failing an ASIC's AC

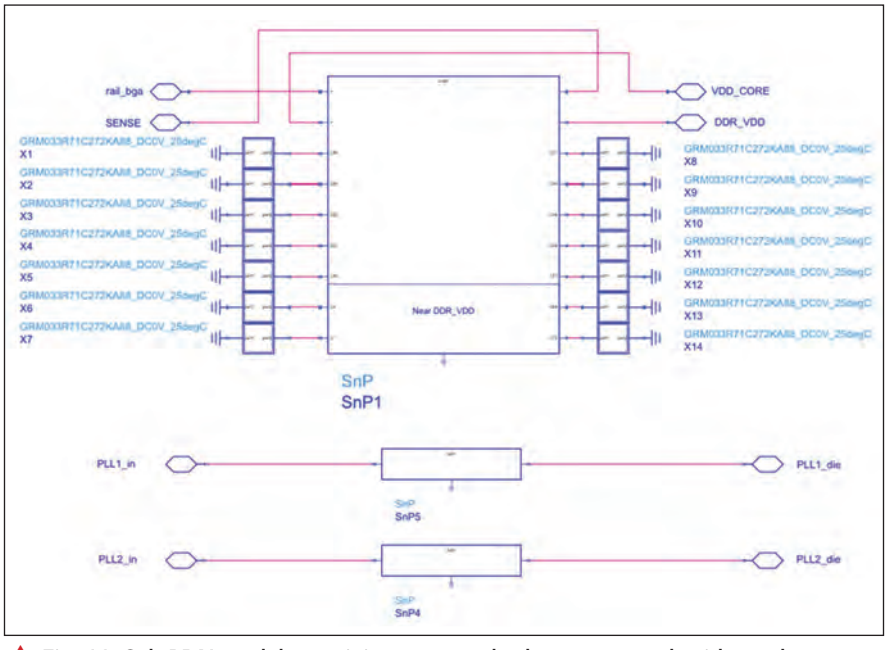


Fig. 11 Sub-PDN model containing extracted substrate artwork with vendor capacitor models.

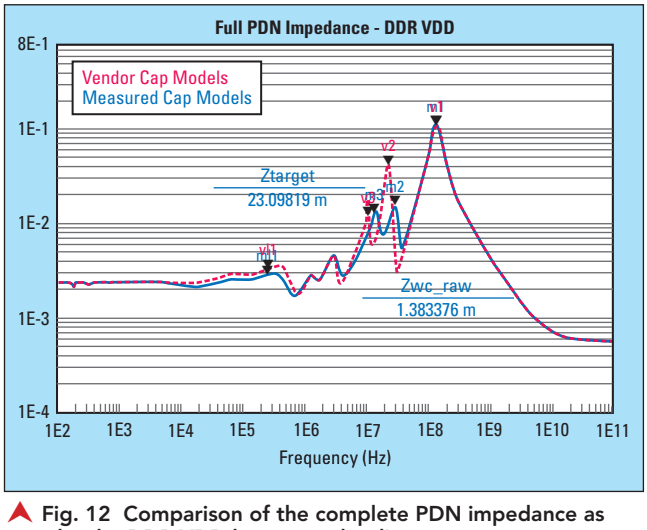


Fig. 12 Comparison of the complete PDN impedance as seen by the DDR VDD bumps at the die.

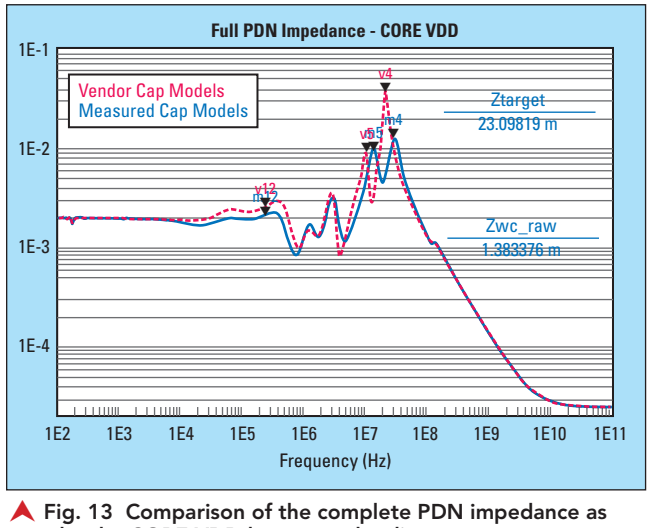


Fig. 13 Comparison of the complete PDN impedance as seen by the CORE VDD bumps at the die.

voltage compliance specification when using a vector-based dynamic current profile from a die model.

Suppose the die models being used for analysis represent vectorless dynamic current profiles. In that case, modulating the load currents at the frequency of the PDN impedance peaks is recommended to address the missing low- and mid-frequency current content in the die model.[9] ***Figure 16*** depicts how the modulation block is added to the system-level simulation. Modulating the die model makes it possible to excite the forced response in a system based on PDN resonances and test for rogue wave conditions.

As summarized in Table 1, with load current modulation at peaks at m2 and m3 on the VDD_DDR PDN (see ***Figure 17***) and at m4 and m5 on the VDD_CORE PDN (see ***Figure 18***), a 98.47 mVpp, or 35.4%, greater voltage ripple is observed. This shows how harmful the additional ESL in vendor capacitor models can impact time domain simulation results.

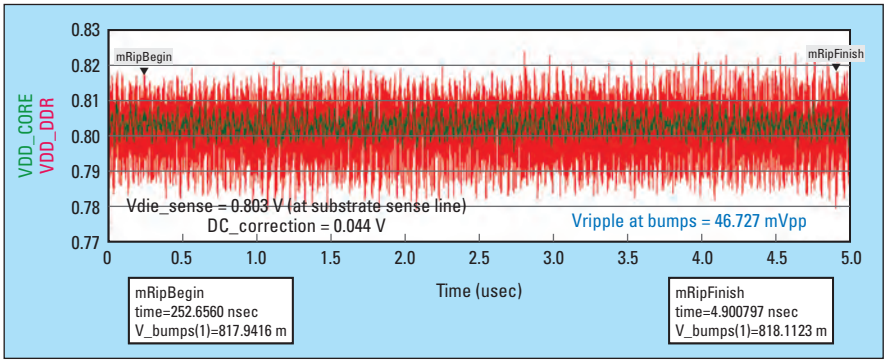


Fig. 14 Voltage ripple with vendor capacitor models.

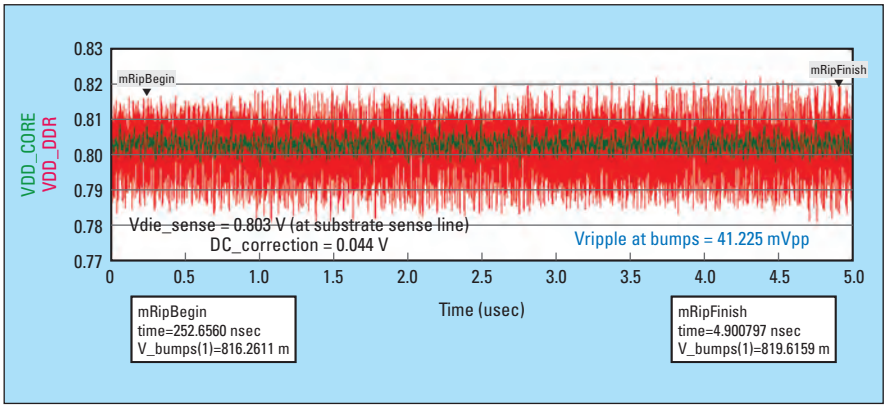


Fig. 15 Voltage ripple with measurement-based capacitor models.

TABLE 1

SUMMARY OF VOLTAGE RIPPLE SIMULATION RESULTS

	Voltage Ripple - No Modulation	*Voltage Ripple – With Modulation*
Vendor Capacitor Models	46.727 mVpp	277.917 mVpp
Measurement-Based Capacitor Models	41.225 mVpp	179.442 mVpp
Delta	5.505 mVpp	98.475 mVpp
Percent Change	11.77%	35.4%

Conclusion

There is no standard method for de-embedding the measurement mount for capacitor models provided by component vendors. Any capacitor model from a vendor may or may not be de-embedded from the PCB mount. Unfortunately, there is often no way to know if a capacitor model includes the PCB mounting inductance beyond making measurement-based models for that capacitor.

As a call to action, vendors should prioritize the improved accuracy of their capacitor models. A standard is needed or, at minimum, designers need to understand how the vendor model was measured. Doing so will enable designers to create faster and more accurate system models, and vendors can benefit by offering products designers can trust. If Vendor A's models certify that they are de-embedded from a fixture mount, whereas Vendor B's models do not specify, a designer will likely select Vendor A's capacitors as a head start on the design analysis.

De-embedded capacitor models must be used for design analysis. Engineers must make their own using an accurate measurement setup if a vendor cannot provide them. It was shown by using measurements

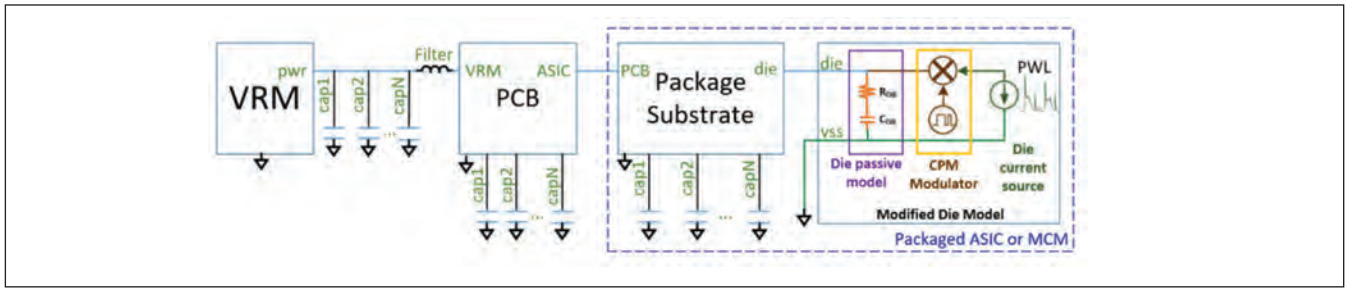


Fig. 16 Power integrity system diagram model with modulated CPM.[9]

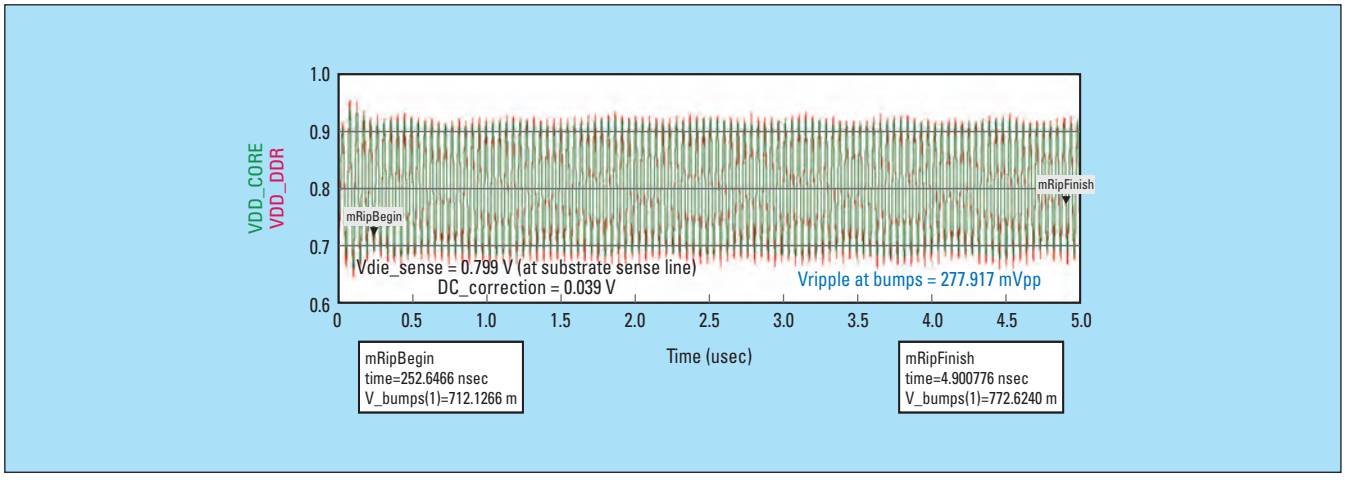


Fig. 17 Voltage ripple with vendor-based models and peak modulation.

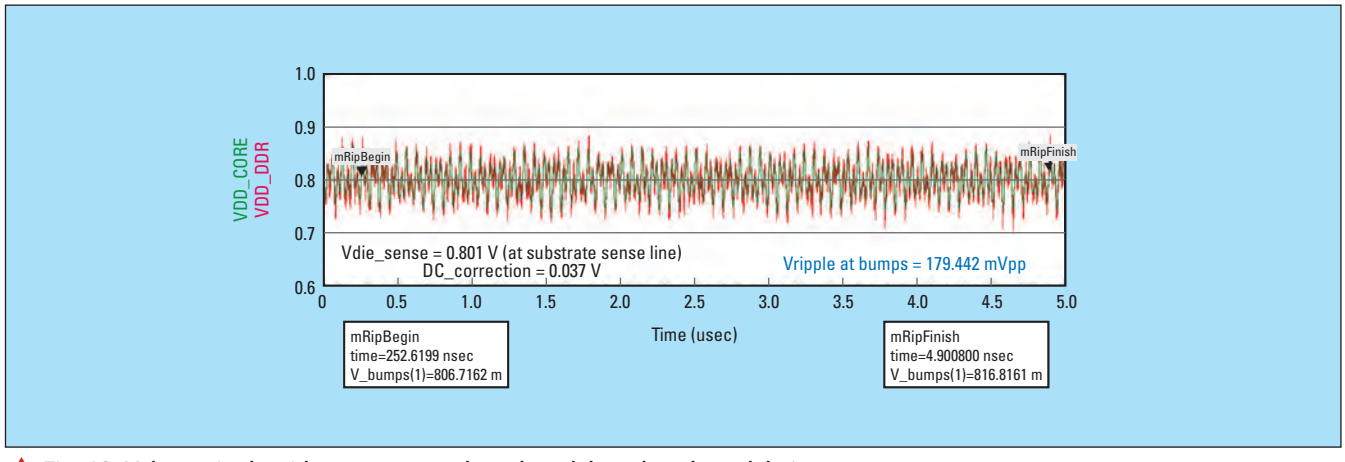
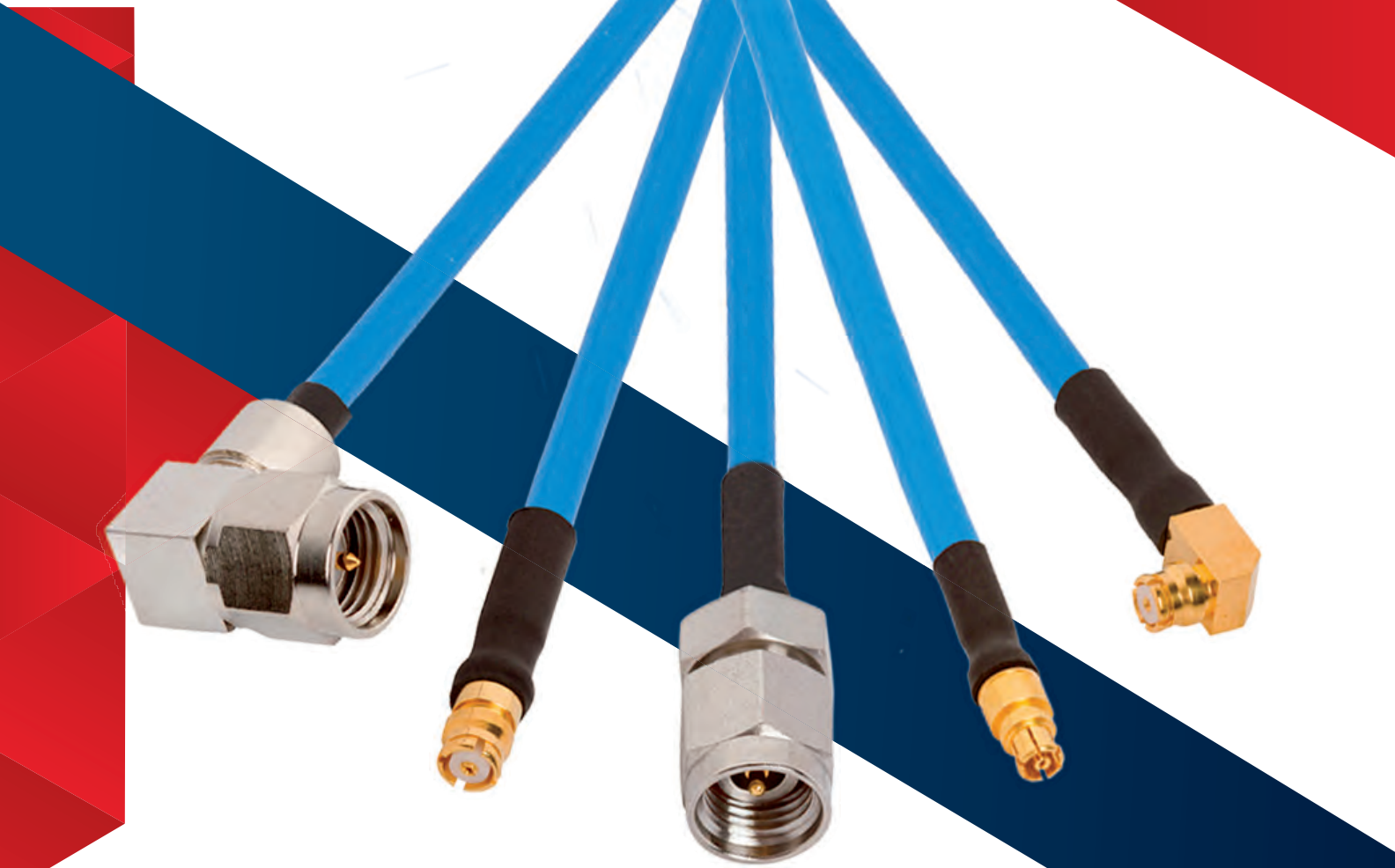


Fig. 18 Voltage ripple with measurement-based models and peak modulation.

without de-embedding the test fixture (typical of many vendor capacitor models) that additional ESL significantly impacts a PDN design analysis in both the frequency domain and time domain. Additional ESL in a capacitor model can lead a designer to over-design the PDN to address these false impedance peaks. To achieve design sign-off for PDNs, simulations must include accurate capacitor models with the PCB mounting inductance removed. If accurate capacitor models are unavailable, designers should be prepared to make their own measurement-based models.■

REFERENCES

1. H. Barnes, "Power Integrity Target Impedance Says it All, Power Delivery is AC not DC," *14th Annual Central PA Center for Signal Integrity Symposium*, Harrisburg, 2021, pp. 1-54.
2. S. Sandler, " Why Full VRM Characterization is Essential," *Signal Integrity Journal*, 2019.
3. S. Sandler, B. Dannan, and H. Barnes, "*Partial Inductance – The Secret to Correlating Simulation and Measurement*," EDICON 2022.
4. S. Sandler, H. Barnes, and B. Dannan, "CHIPHEADS, Hands-On PDN Impedance and Calibration Basics," *DesignCon, 2023*.
5. S. M. Sandler, "Extending the Usable Range of the 2-port Shunt through Impedance Measurement," *IEEE MTT-S Latin America Microwave Conference*, Dec. 2016, pp. 1–3.
6. B. Dannan and S. Sandler, "Calibrating the 2-Port Probe for Low Impedance PDN Measurements," *Signal Integrity Journal, 2021*.
7. Keysight PathWave PIPro, Web: https://www.keysight.com/us/en/product/W3034E/pathwave-pipro.html.
8. P. J. Pupalaikis, "*S-Parameters for Signal Integrity*," Cambridge: Cambridge University Press, 2020.
9. B. Dannan, J. Kuszewski, et al., "*Improved Methodology to Accurately Perform System Level Power Integrity Analysis Including an ASIC die*," DesignCon, 2022.
10. S. Sandler, B. Dannan, H. Barnes, C. Yots, "*VRM Modeling and Stability Analysis for the Power Integrity Engineer*," DesignCon, 2023.
11. S. Sandler, "Designing Power for Sensitive Circuits," *Signal Integrity Journal, 2017*.
12. *Picotest J2113A Semi-Floating Differential Amplifier, Web:* https://www.picotest.com/products_J2113A.html.
13. *Picotest Omicron Lab Bode 100 VNA, Web:* https://www.picotest.com/products_BODE100.html.
14. *Picotest PDN Cables*, Web: https://www.picotest.com/pdn-cable.html.
15. Analog Devices *LTM4650-2 Dual 25A or Single 50A µModule Regulator,* Web: https://www.analog.com/en/products/ltm4650-2.html.
16. *Cadence Voltus IC Power Integrity Solution*, Web: https://www.cadence.com/en_US/home/tools/digital-design-and-sign-off/silicon-sign-off/voltus-ic-power-integrity-solution.html.



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Worst-Case Bit-Pattern Generator for Eye Diagram Analysis of Non-LTI High-Speed Channels

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With the exponential increase of the data rate in high-speed channels, their evaluation using an eye diagram simulation has become more cumbersome. This task is especially challenging for non-LTI systems, where statistical methods are not applicable and a long transient simulation with a random bit pattern is necessary. Therefore, we propose a machine learning approach based on Bayesian Optimization that creates an optimized bit pattern to maximize the ISI, resulting in faster convergence of eye diagram analysis. In addition, crosstalk, random noise, random jitter, and other types of interference can be added to the analysis. Numerical results demonstrate up to 14x speedup and more accurate results compared to the conventional eye diagram analysis.

Performance of high-speed Serializer/deserializer (SerDes) channels is often evaluated using an eye diagram. The conventional eye diagram is simulated with a lengthy transient simulation and a random bit pattern source (i.e., transient eye). However, for modern channels where the bit error rate (BER) is required to be 10^{-12} or less, the simulation would be very time-consuming. Therefore, we propose taking advantage of modern machine learning techniques to generate an optimized bit pattern and use it in place of the random bit pattern, where the optimized bit pattern is significantly shorter. The bit pattern is optimized to maximize the inter-symbol interference (ISI), which refers to interference of a single bit response with neighboring symbols.[1] Since ISI can span over many unit intervals (UIs) for modern channels, many combinations of this effect can exist; therefore, a significantly long random transient simulation would be necessary to capture the correct eye opening. However, by optimizing the bit pattern to converge to the most challenging waveforms, the eye opening is found with a significantly shorter transient simulation. ***Figure 1*** illustrates the general topology of a PCIe link, which is an example of modern SerDes channels.

Statistical eye diagrams have been developed to avoid expensive transient simulation. This includes Peak Distortion Analysis[2] and StatEye.[3] However, unlike the proposed approach, they are only applicable to linear time-invariant (LTI) systems. Furthermore, parametric surrogate models of high-speed channels have been proposed in the literature.[4,5] However, these methods require a dataset of existing designs with variations of design parameters for training. In addition, training a surrogate model can limit accuracy. In contrast, the proposed approach in this article does not require an initial dataset and the optimization is performed with adaptive dynamic sampling. Additionally, the proposed approach works with accurate short time domain simulations, and it does not suffer from the loss of accuracy caused by surrogate models. A survey of other eye estimation methods and their respective

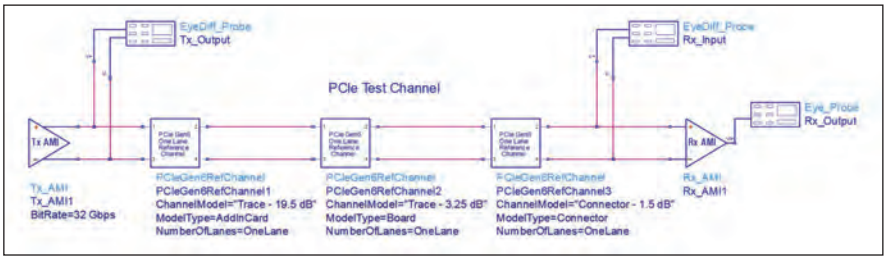

Fig. 1 PCIe topology.

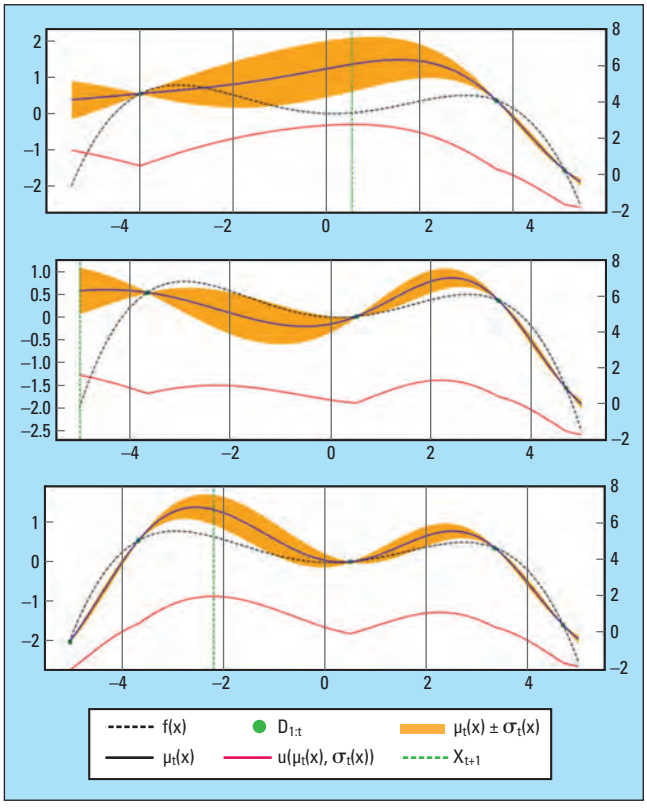

Fig. 2 First three iterations of BO on a 1D test function.

limitations is provided by Dolatsara.[6]

Recently, a novel method known as the Worst-Case Eye analysis was introduced.[7] This methodology is designed to alter the bit sequence in a way that intensifies ISI and yields eye height, eye width, and the contour of the eye opening. In the present study, we expand upon this methodology. The significant enhancement involves producing the worst-case bit pattern rather than the eye metrics. Leveraging this progression, we have been able to perform a faster and more accurate eye diagram simulation compared to the traditional transient eye. It also has enabled us to incorporate various types of noise and jitter into the worst-case eye diagram. Additional steps are also taken to improve the optimization in Dolatsara, et al.[7], including a new way of handling discrete variables, avoiding repeated samples, and the normalization of objective functions. The proposed approach is henceforth termed the Worst-Case Bit-Pattern Generator (WCBPG). WCBPG has been recently released with Keysight Advanced Design System (ADS) 2024 Update 1.0.[8]

Background Review

In this section, Gray code mapping and Bayesian optimization (BO), which were used in the development of WCBPG, are reviewed.

Gray Code Mapping

The reflected binary code, or the Gray code, is a reordering of the binary numbers so that each two subsequent numbers only differ in a single binary digit. For instance, in a two-bit system, the binary numbers are {00, 01, 10, 11}. Gray code maps this sequence to {00, 01, 11, 10}[9]. Gray code is used in WCBPG to map the possible bit patterns to a space that is easier to optimize. This is discussed further later in this article.

Bayesian Optimization

BO is a dynamic optimization technique in machine learning applicable to nonlinear and nonconvex functions. It is especially effective for optimization of functions that are costly to evaluate, thanks to its economical use of samples and fast convergence. It is an iterative algorithm based on the Bayes theorem.[10] ***Figure 2*** illustrates three iterations of BO for maximization of a one-dimensional (1D) test function. f(x) represents the unknown objective function, which has been sampled at $D_{1:t}$, with t being the current iteration. Furthermore, Gaussian Process (GP) is used for modeling f(x), which is shown by $N(\mu_t(x),\sigma_t^2(x))$ representing a normal distribution for f(x) at every point, with mean equal to μ_t and variance equal to σ_t^2. It represents where the model expects f(x) to appear. Moreover, the acquisition function, $u(\mu t(x),\sigma_t(x))$, is used to balance exploration and exploitation and find the next sample for evaluation, which is most likely to converge toward the global maximum. Note that $u(\mu_t(x),\sigma_t(x))$ is plotted on a different scale shown on the right side of each plot. It illustrates a given score for each possible future sample. The maximum of this analytical function is marked and shows the next sampling point, x_{t+1}. The algorithm repeats until reaching a preset limit and updates GP based on the new observations. Finally, it reports the maximum found sample. For mathematical details including the Gaussian Process and the acquisition function, see Brochu, et al.[10]

The Proposed Worst-Case Bit-Pattern Generator (WCBPG)

Jitter and noise are affected by the memory effect and the bit pattern sequence in high-speed channels. We show a partial bit pattern surrounding the current symbol (i.e., current bit) as:

$$\lambda = \left[\lambda_{-n},\lambda_{-n+1},\cdots,\lambda_{-1},\lambda_0,\lambda_1,\cdots,\lambda_m\right] \quad (1)$$

where λ_0 is the current transmitted symbol, λ_{-1} to λ_{-n} are the previous symbols with non-negligible post-cursors in ISI, and λ_1 to λ_m are the future bits causing the non-negligible pre-cursors in ISI. WCBPG optimizes

λ to achieve the worst-case eye (WCE) opening. WCE is defined as the eye with the smallest eye height (EH) and eye width (EW), since these two measures are often used as the major metrics to compare the eye diagrams. Currently, the proposed approach supports the non-return-to-zero (NRZ) signal; however, the following methodology can be easily extended to PAM-n. As shown in ***Figure 3***, for the NRZ signal, EH is the difference between the lowest received high symbol and the highest received low symbol. On the other hand, EW is UI minus the peak-to-peak jitter (PPJ), where PPJ is the difference between the rightmost zero-crossing and the leftmost zero-crossing, where zero-crossing is defined as the time point when a rising or falling edge passes through the threshold voltage differentiating the high and low logics. This breaks down finding the WCE into six smaller optimization problems, which are finding the lowest high voltage (V_{LH}), highest low voltage (V_{HL}), rightmost rising edge zero-crossing time (t_{RR}), rightmost falling edge zero-crossing time (t_{RF}), leftmost rising edge zero-crossing time (t_{LR}), and leftmost falling edge zero-crossing time (t_{LF}) as a function of λ, which we call the worst-case points.

The optimization space in the problems above is high-dimensional due to the large n in modern channels. It is also discrete and sparse since λ_i can only take zero or one values. This results in challenging optimization problems. Therefore, we use our knowledge of high-speed channels to simplify the optimization. For the problems considered in this article, m is fixed at 1 since further pre-cursors are negligible. Moreover, $[\lambda_{-1},\lambda_0,\lambda_1]$ are set intuitively for each optimization problem based on the behavior common to high-speed channels. For instance, for the lowest high, these three symbols are always set to [0,1,0]. Furthermore, a decimal number equivalent to $[\lambda_{-n},\lambda_{-n+1},\ldots,\lambda_{-2}]$ is generated, where λ_{-n} is the least significant bit (LSB), and λ_{-2} is the most significant bit (MSB). We call this number the index of each possible bit pattern. The optimization is now converted to a 1D problem where the index number corresponding to the worst-case points needs to be found. Note that for ISI, λ_{-n} is the least effective symbol since it is the furthest from the current symbol. Therefore, by choosing λ_{-n} as the LSB, the variation in ISI for adjacent bit patterns is relatively gradual. However, adjacent binary digits can be significantly different or even completely opposite in the binary domain. Therefore, we use the Gray code mapping to reorder the bit pattern indices and create smoother objective functions. In conclusion, the optimizer needs to solve the following optimization problems:

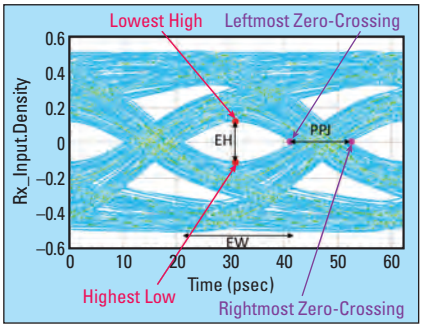

Fig. 3 EH and EW on a sample eye diagram and their calculation using lowest high, highest low, and leftmost and rightmost zero-crossing points.

$$
\begin{aligned}
V_{LH} &= \min_{lg} V\left(t_s, I_g, (\lambda)\big|_{\lambda_{-1}=0,\lambda_0=1,\lambda_1=0}\right)\\
V_{HL} &= \max_{lg} V\left(t_s, I_g, (\lambda)\big|_{\lambda_{-1}=1,\lambda_0=0,\lambda_1=1}\right)\\
t_{RR} &= \max_{lg} t\left(V_0, I_g, (\lambda)\big|_{\lambda_{-1}=0,\lambda_0=1,\lambda_1=0}\right)\\
t_{RF} &= \max_{lg} t\left(V_0, I_g, (\lambda)\big|_{\lambda_{-1}=1,\lambda_0=0,\lambda_1=1}\right)\\
t_{LR} &= \min_{lg} t\left(V_0, I_g, (\lambda)\big|_{\lambda_{-1}=0,\lambda_0=1,\lambda_1=1}\right)\\
t_{LF} &= \min_{lg} t\left(V_0, I_g, (\lambda)\big|_{\lambda_{-1}=1,\lambda_0=0,\lambda_1=0}\right)
\end{aligned}
\qquad (2)
$$

where $V(t_s,I_g(\lambda)|\lambda_{-1}=.,\lambda_0=.,\lambda_1=.)$ is the output voltage at t_s, when the bit pattern corresponds to the Gray code index I_g, and $t(V_0,I_g(\lambda)|\lambda_{-1}=.,\lambda_0=.,\lambda_1=.)$ is the time when the desired rising/falling edge passes the threshold voltage V_0, when the bit pattern corresponds to the Gray code index I_g. PPJ is calculated as $\max(t_{RR},t_{RF}) - \min(t_{LR},t_{LF})$. ***Figure 4*** illustrates a snapshot of optimization of V_{HL} in a test case, in the same format as Figure 2.

In this work, finding a maximum with BO is implemented in C++, and finding a minimum is achieved by finding the maximum of negative of the objective function. The following steps are taken to improve performance of BO compared to Dolatsara, et al.[7] Conventional BO is designed for optimization of continuous variables. In Dolatsara, et al.[7] BO samples were simply rounded to the nearest integer; however, this can degrade the performance. In WCBPG, BO is adapted by modifying the sample space of the acquisition functions. In this approach, unlike the conventional BO, the acquisition function is only evaluated at a bag of random integer samples. Then, the sample with the

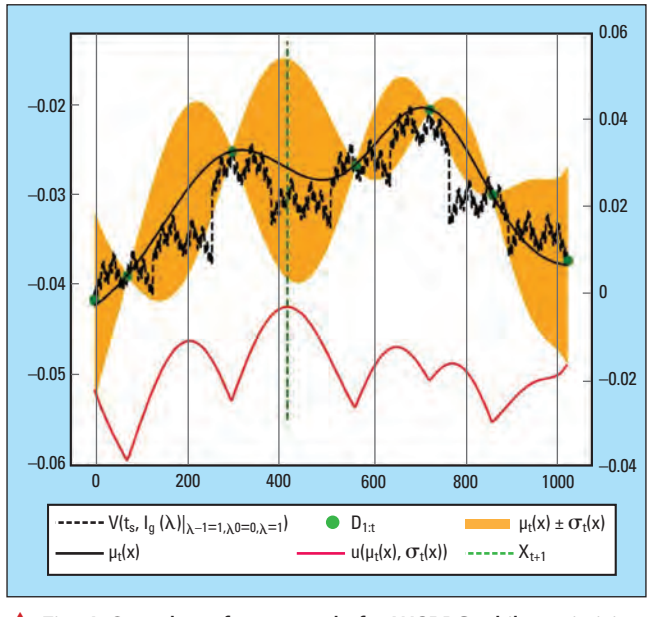

Fig. 4 Snapshot of an example for WCBPG while optimizing V_{HL}.

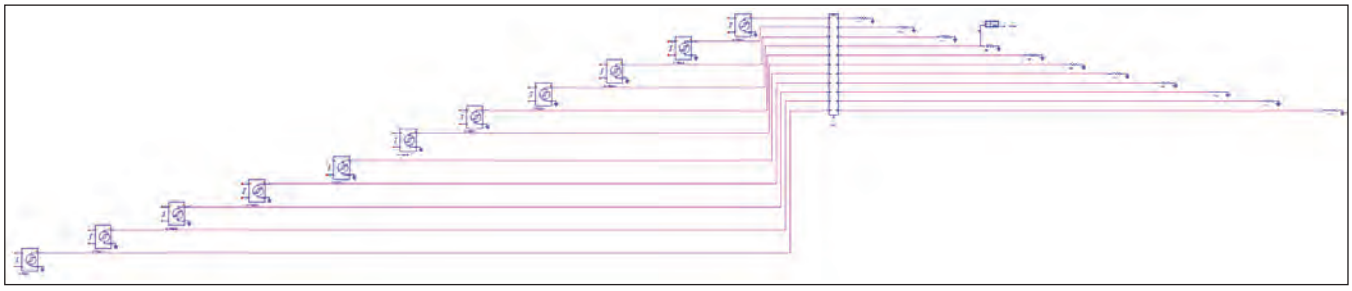

Fig. 5 The high-speed channel considered in example 1.

highest score is selected to be evaluated at the next iteration to update the Gaussian Process model. To avoid reselecting the same samples, at the beginning of each iteration, we remove the samples that we have evaluated so far from the bag of samples given to the acquisition function. Therefore, we do not consider them when looking for the next sample. Furthermore, V_0 and t_s in Equation (2) are calculated as:

$$V_0 = \frac{V_{max} + V_{min}}{2} \tag{3}$$

$$t_s = \frac{\min\left(t_{LF}, t_{LR}\right) + \max\left(t_{RF}, t_{RR}\right)}{2} + \frac{UI}{2} \tag{4}$$

where V_{max} and V_{min} are the maximum and minimum received voltages, respectively. Moreover, hyperparameters of BO can differ from one example to another. To avoid resetting these parameters for each test case, we normalize the objective functions in Equation (2), using V_{max} and V_{min} for voltage functions and the unit interval for time functions. Next, the bit patterns equivalent to the indices found in Equation (2) are constructed. After adding some zero-padding, these bit patterns are concatenated and written into a file; then, the result is fed to a transmitter and used for eye diagram simulation. Finally, random noise and jitter and other types of distortion are added to the transmitter's output as usual.

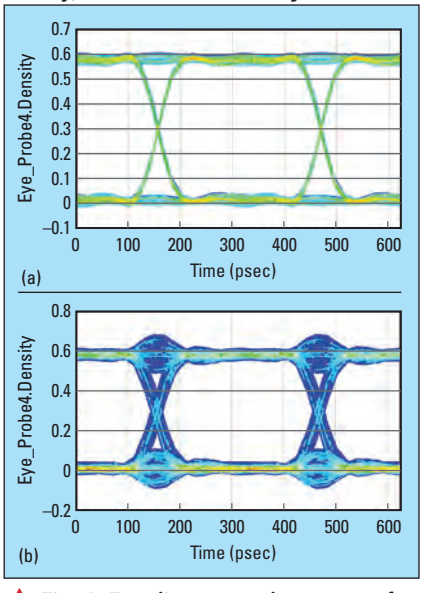

Fig. 6 Eye diagram at the output of example 1, using a) conventional transient eye and b) the proposed WCBPG.

Numerical Examples

Example 1

To evaluate performance of WCBPG, the channels shown in ***Figure 5***, which are taken from a DDR4 DIMM system, are considered. It includes 11 coupled channels, input sources, and 50 Ω terminations. It operates at 3.2 Gbps. V_{high} and V_{low} of the transmitter are set to 1.2 V and 0.0 V, respectively. Initially, all the sources transmit random patterns. We focus on the analysis of the fourth channel from the top. The eye diagram is measured before the termination. ***Figure 6a*** illustrates the conventional eye diagram of this channel, which is performed with 100,000 random bits; its specific metrics are provided in ***Table 1***.

TABLE 1
COMPARISON OF EYE DIAGRAM ANALYSIS APPROACHES IN EXAMPLE 1

	Transient Eye	*WCBPG*
Eye Height at 312.5 ps	513 mV	509 mV
Eye Width at 0.3 V	307 ps	290 ps
Number of UIs	100,000	1000
Total Sim. Time	1054 s	73 s

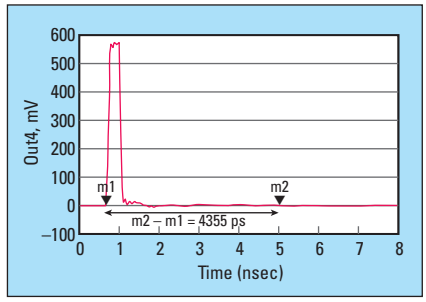

Fig. 7 Single bit response of the channel in example 1.

Next, we utilize the proposed WCBPG to create the worst-case bit pattern for this channel. *n* in Equation (1) is set to 13, based on the single bit response of this channel in absence of crosstalk as shown in ***Figure 7***; however, crosstalk is present when the bit pattern is being generated. Moreover, the number of iterations for optimizing each objective function in Equation (2) is set to 25. We use the bit pattern generated by WCBPG to run a transient simulation for the length of 1000 UIs. Therefore, we run through the generated bit pattern multiple times, which is done so for practical reasons. The resulting eye diagram analysis results are presented in ***Figure 6b*** as well as Table 1, which shows a smaller eye opening compared to the transient eye. Note that in this context, smaller is more accurate because the eye diagram in Figure 6b is actually derived from a transient simulation with an optimized bit pattern. The total simulation time of this approach is 73 seconds, which includes the BO and generation of the worst-case bit pattern. Therefore, it provides an increase in speed of roughly 14x compared to the conventional eye diagram analysis, while the results are considerably more ac-

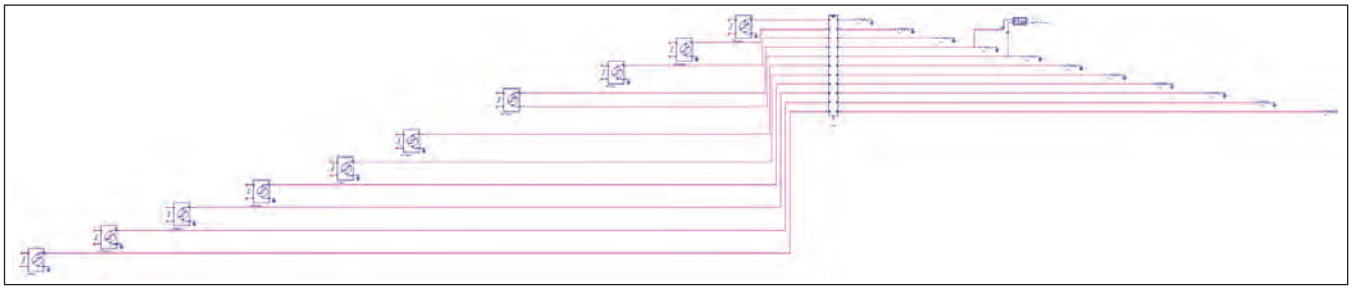

Fig. 8 The high-speed channel considered in example 2.

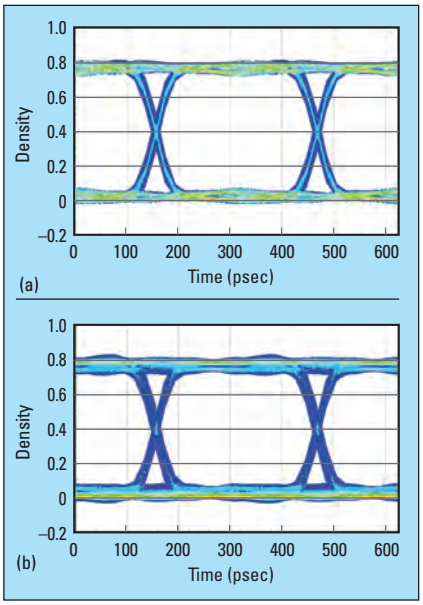

Fig. 9 Eye diagrams at the output of example 2, using a) conventional transient eye and b) the proposed WCBPG.

curate.

Example 2

In this example, we have modified the system in example 1 by creating a differential channel using the fourth and fifth channels from the top and measuring the differential corresponding output, as shown in ***Figure 8***. In addition, random jitter (RJ) and sinusoidal periodic jitter (PJ) have been added to this channel's transmitter. Standard deviation of RJ is set to 1 ps. PJ's amplitude and frequency are 2 ps and 100 MHz, respectively. The rest of the parameters stay the same. The conventional eye diagram using 100,000 random bits is illustrated in ***Figure 9a***. In addition, the eye metrics are summarized in ***Table 2***. For WCBPG, *n* in Equation (1) is set to 16 based on the single bit response of this channel in absence of crosstalk, as shown in ***Figure 10***; however, crosstalk is present when the bit pattern is being generated. Moreover, the number of iterations for optimization of each objective function in Equation (2) is set to 30. The worst-case bit pattern is generated with no RJ and PJ to maximize ISI. Next, RJ and PJ are turned on, and a transient simulation for the length of 10,000 UIs is performed using the created bit pattern. We have increased the length of this simulation to 10,000 UIs because it includes RJ and PJ. Since WCBPG does not optimize for RJ and PJ, we need to increase the length of the simulation to observe their effects; however, the total simulation time would be much shorter than the entirely random transient eye. The resulting eye diagram analysis results are presented in ***Figure 9b*** and Table 2, showing a smaller eye opening than the transient eye. As discussed before, this shows the WCBPG results in a more accurate eye diagram, even in the presence of RJ and PJ. In addition, the results are generated 5.75x faster than the transient eye.

TABLE 2

COMPARISON OF EYE DIAGRAM ANALYSIS APPROACHES IN EXAMPLE 2

	Transient Eye	*WCBPG*
Eye Height at 312.5 ps	647 mV	635 mV
Eye Width at 0.4 V	297 ps	294 ps
Number of UIs	100,000	10,000
Total Sim. Time	1093 s	190 s

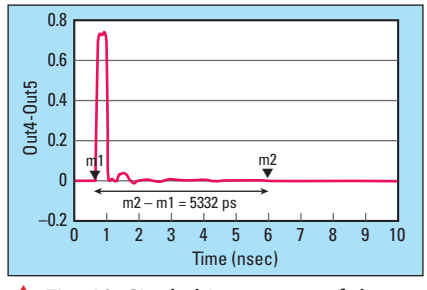

Fig. 10 Single bit response of the channel in example 2.

Conclusion

In this article, WCBPG is introduced to create a bit pattern for faster eye diagram analysis of high-speed channels. The pattern generated by WCBPG utilizes Bayesian Optimization to maximize ISI; moreover, it takes advantage of the Gray code mapping to create smoother objective functions. Numerical examples show that the proposed approach demonstrates a superior performance compared to conventional eye analysis, even in the presence of crosstalk, RJ, and PJ.

REFERENCES

1. M. P. Li, *Jitter, Noise, and Signal Integrity at High-Speed*, Upper Saddle River, NJ, Prentice Hall, 2007.
2. B. K. Casper, M. Haycock, and R. Mooney, "An Accurate and Efficient Analysis Method for Multi-Gb/s Chip-to-chip Signaling Schemes," in *IEEE Symp. Very Large Scale Integr. (VLSI) Circuits*, 2002.
3. A. Sanders, M. Resoo, and D. Ambrosia, "Channel Compliance Testing Using Novel Statistical Eye Methodology," *DesignCon*, 2004.
4. T. Lu, J. Sun, K. Wu, and Z. Yang, "High-Speed Channel Modeling With Machine Learning Methods for Signal Integrity Analysis," *IEEE Transactions on Electromagnetic Compatibility*, Vol. 60, No. 6, 2018, pp. 1957-1964.
5. Y. Choi, P. Kashyap, W. Sun, M. S. Chughtai, C. Cheng, and P. Franzon, "Data-driven PAM4 SerDes Modeling with Generative Adversarial Network," *DesignCon*, 2023.
6. M. Ahadi Dolatsara, "High-Speed Channel Analysis and Disign Using Polynomial Chaos Theory and Machine Learning," *Doctoral dissertation, Georgia Institute of Technology*, 2021, pp. 8–14.
7. M. Ahadi Dolatsara, J. A. Hejase, W. D. Becker, J. Kim, S. K. Lim, and M. Swaminathan, "Worst-case Eye Analysis of High-speed Channels based on Bayesian Optimization," *IEEE Transactions on Electromagnetic Compatibility*, Vol. 63, No. 1, Feb. 2021,pp. 246–-258.
8. "PathWave Advanced Design System (ADS)," Keysight Technologies, Web: https://www.keysight.com/us/en/products/software/pathwave-design-software/pathwave-advanced-design-system.html. [Accessed 3 November 2023].
9. H. S. Wilf, "Combinatorial Algorithms: An Update," Philadelphia, PA, SIAM, 1989.
10. E. Brochu, V. M. Cora, and N. de Freitas, "A Tutorial on Bayesian Optimization of Expensive Cost Functions, with Application to Active User Modeling and Hierarchical Reinforcement Learning," *arXiv:1012.2599*, 2010.

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REFLECTIONS

DesignCon Returns to Celebrate Engineers and Innovation

Suzanne Deffree
Group Event Director, DesignCon

DesignCon, the premier high-speed communications and system design conference, returns to its home at the Santa Clara Convention Center in Santa Clara, Calif., with technical paper sessions, tutorials, industry panels, product demos, and exhibits, January 30 to February 1, 2024.

Education Highlights

DesignCon's conference program covers all aspects of electronic design, including signal and power integrity, high-speed link design, and machine learning.

DesignCon attendee interests continue to be strongest in optimizing high-speed link design, boasting the highest 2023 event attendance and also holding the highest number of paper submissions for 2024. The number of paper submissions for the upcoming conference is usually a good indicator of research activity and overall interest. For 2024, we have seen the next highest number of submissions for the core topics of modeling, analysis, and optimization of interconnects.

Following are some of the highest-rated sessions by DesignCon's Technical Program Committee peer reviewers for the upcoming 2024 event:

"Considerations for Achieving 200 Gbps Signaling per Electrical Lane Over 1 Meter of Twinaxial Copper Cable" is a combined effort from Alphawave Semi, Amphenol, Cisco Systems, Keysight Technologies, MC Communications, PHY-SI, Rohde & Schwarz, and Samtec. This is expected to be important research for the continued evolution of IEEE 802.3 Ethernet specs.

"Design, Simulation & Validation Challenges of a Scalable 2000 Amp Core Power Rail" from Broadcom Semiconductors, Monolithic Power Systems, Keysight Technologies, PICOTEST, and Signal Edge Solutions should provide a good mix of design, simulation, and measurement validation. It will be particularly helpful that the authors plan to offer correlation to real hardware.

"224-Gbps MLSD Receiver Simulations & Correlations with OIF-CEI-224G/802.3dj COM Methodology" from Intel plans to provide both implementation of MLSD in the simulation flow and correlation with COM script. The session is expected to include a clear reason for using MLSD for receiver equalizer optimization for higher data rates and longer reach interconnects.

"Physics-Based Via to Stripline Model for Systematic Link Simulation on Multilayer Cavities Up to 100 GHz" is from the EMC Lab at Missouri University of Science and Technology. It's beneficial to have a physics-based analytical formula to calculate the impedance of via-trace transition rather than getting results from full wave simulation. If the paper's claims come through, this could be a great contribution to the industry.

"A Novel PCB Footprint for Double-Sides Stacked Optical Module Application" comes from Cisco. Footprints have a huge impact on performance, and very often they are dictated by mechanical restrictions. Optimizing footprints isn't done properly by many companies, so this information could have a beneficial impact on the DesignCon community.

"Automotive High-Speed Serial: How the Harsh Environment Challenges Established Technology & Test Methods" from Valens Semiconductor and BitifEye Digital Test Solutions aims to address design, diagnostic, and compliance testing methodologies required to ensure durable, error-free automotive communication links composed of interoperable components through the vehicle lifespan. Discussion of the requirements of the current HSS automotive standards will be included.

"Panel – Test on Wheels: T&M for Automotive Standards" will bring attendees up-to-date on how the automotive industry is solving the signal integrity challenges of this uniquely noisy, hot/cold, wet/icy/smoky, and violent environment. Now in its third year, the panel will include engineers from BMW, Keysight, and other leaders.

Attendee Pass Information

In total, DesignCon 2024 is offering more than 120 educational sessions. Conference passholders will continue to have access to the 14 tracks of education, with more than 85 sessions curated by our 97-person Technical Program Committee. Additionally, DesignCon has expanded its Drive World conference from eight sessions to 20+ sessions, focused on engineering in the autonomous and electric vehicle industries. Supporting DesignCon's Drive World education will be a dedicated Advanced Automotive section of the expo floor, hosting suppliers with a specific focus on automotive and energy storage design.

Additionally, all attendees have access to daily keynotes, panels, Chiphead Theater presentations, exhibitor-led education, the Engineer of the Year and Best Paper Awards presentations, and the DesignCon expo floor.

Among 150+ exhibitors, DesignCon's expo floor will present some of the industry's most influential companies, including host sponsor Amphenol, Cadence, Keysight, Molex, Mouser, Samtec, TE Connectivity, and more. Experts from these companies will be on-site to answer design questions, provide advice on engineering, and present educational demonstrations on the latest in high-speed design tools, technologies, and developments.

New in 2024, DesignCon launches its 40 Under 40 program, celebrating 40 up-and-coming engineers. These engineers will be recognized ahead of and at the event as rising stars, and will receive access to all DesignCon education in Santa Clara, in addition to the expo floor offering an exclusive breakfast with industry leading expert engineers and mentors.

Further Information

DesignCon's 2024 exhibition is open Wednesday and Thursday, January 31 and February 1, and the conference is presented Tuesday, Wednesday, and Thursday, January 30-Februaury 1. Registration is open now. More information on the full event is available on DesignCon.com.

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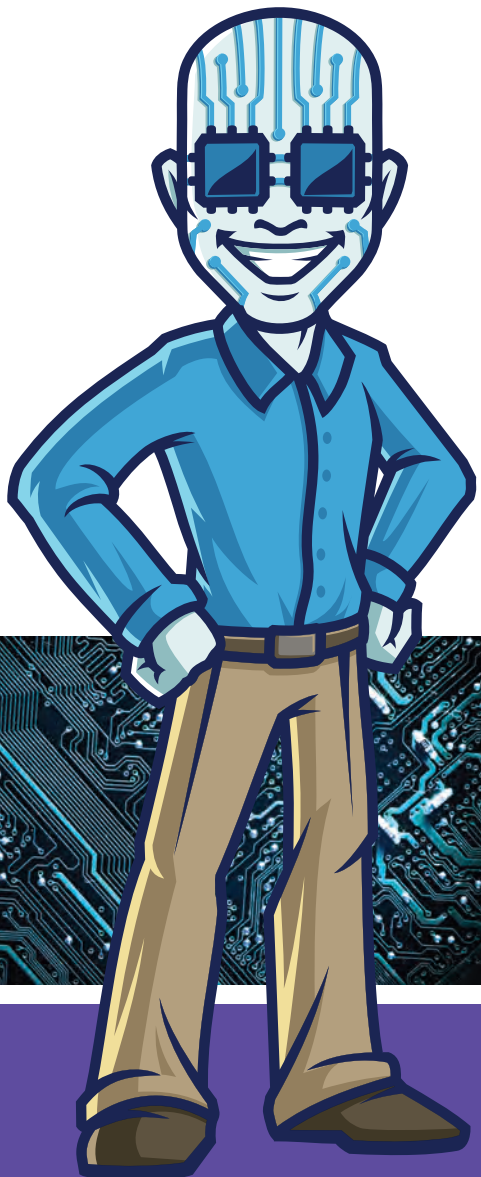

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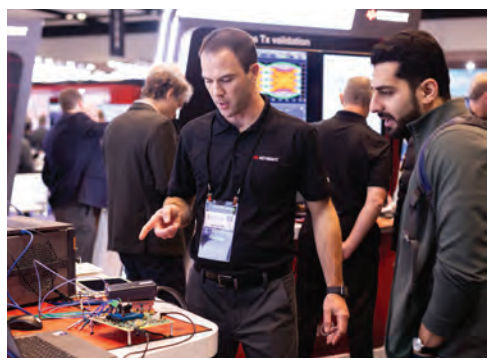

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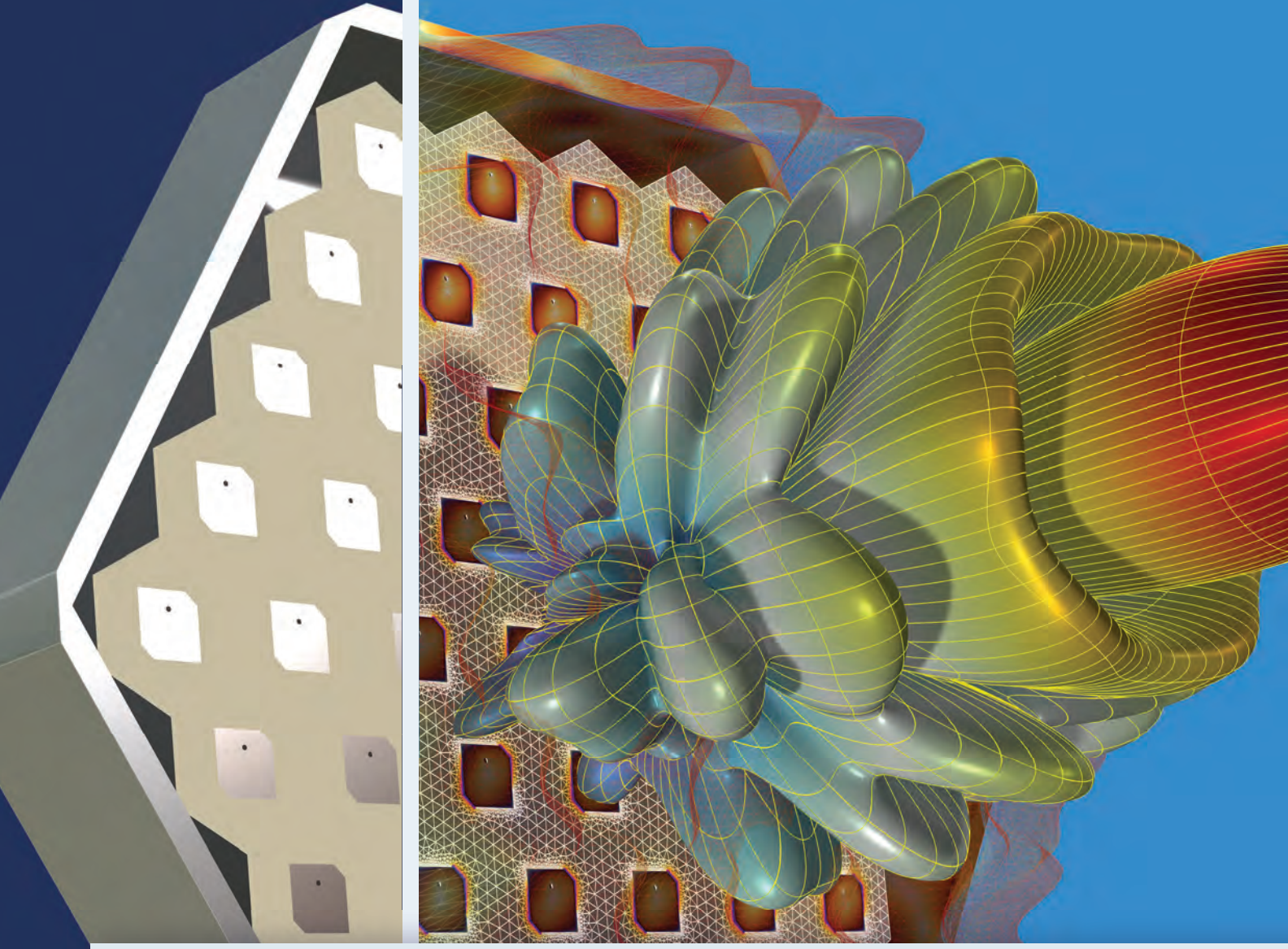

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