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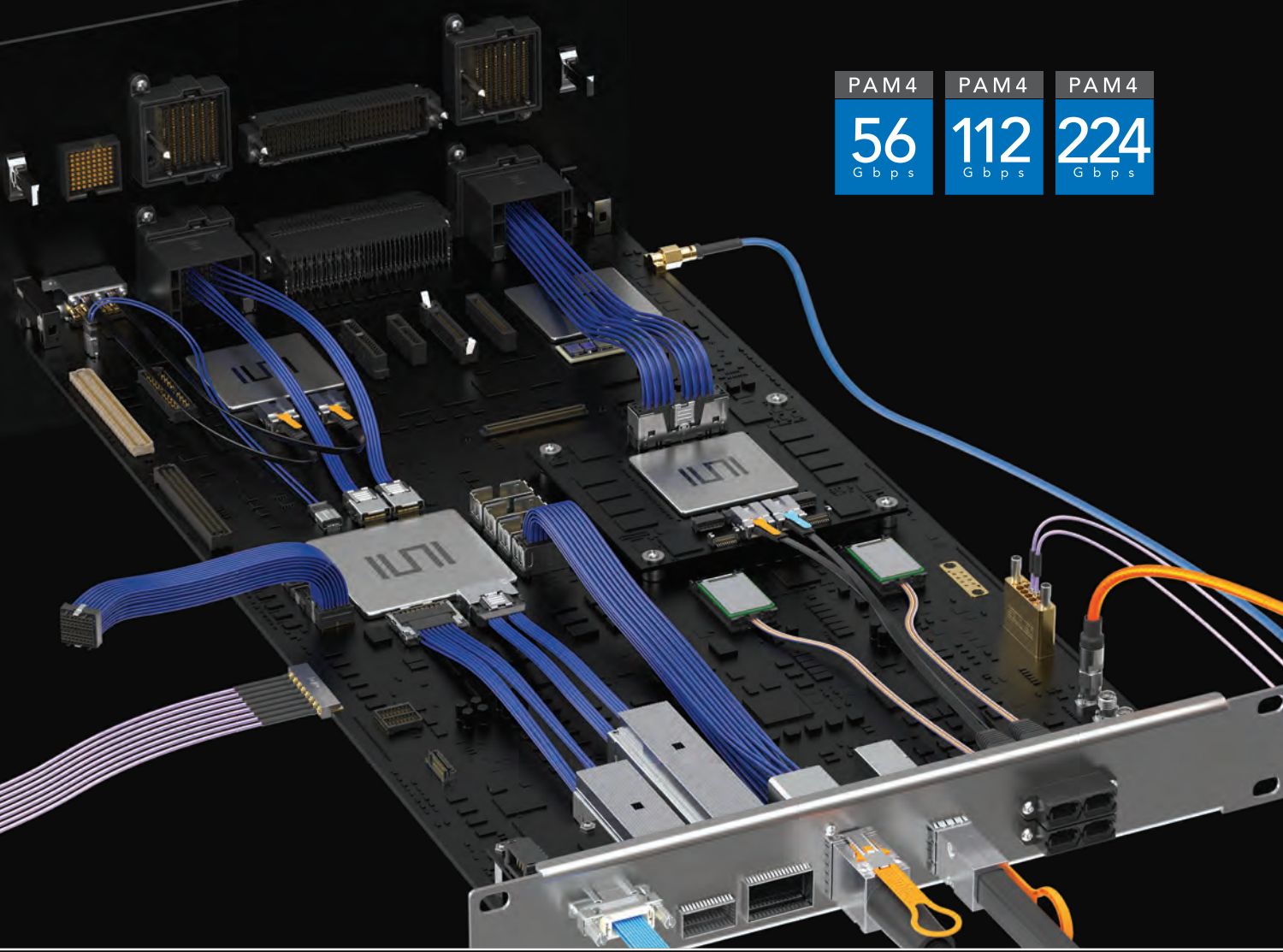

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The Need for Speed and the Cost in Power

Eric Bogatin, Technical Editor
Signal Integrity Journal

Our economy is both fueled and limited by energy sources. Before the Industrial Revolution, human strength and ability were supplemented by animals. We still retain a measure of power in terms of the ability of a horse. One horsepower (hp) is equivalent to about 750 W, which is about 5x what one person can deliver.

The Industrial Revolution, which began in 1760, was distinguished by the introduction of energy sources that offered even more power than a horse. Initially, power was supplied using wind and water, until the switch was made to steam, wood, coal, and eventually, oil.

However, the transfer of energy from the source to the action was through a mechanical linkage. This meant that the application was always in proximity to the engine. Mills were located next to water sources. Trains carried their fuel and steam engines with them.

Electrification introduced a new era when the conversion of power from its raw source into an easily transportable form allowed the use of the energy remotely. Thomas Edison's first DC power station on Pearl Street in New York City came online in 1882, delivering 100 kW. By 1896, Westinghouse's Niagara Falls AC power station came online, delivering 37 MW of power. The need for electric power was driven by the light bulb and the streetcar.

Fast forward to today and the power consumption of the electronics industry. What is fueling this growth is the introduction of artificial intelligence (AI)/machine learning processing in data centers.

According to a report released in 2024 by Newmark, 5% of the data center applications in 2021 were for AI applications. By 2025, 30% of the applications in data centers will be for AI. Capex spending by the companies creating large data centers has a compound annual growth rate of 30%.

AI processing is notoriously power-hungry. The same Newmark report says the typical power consumption of a rack in a data center has been about 12 kW, while an AI processor rack consumes as much as 50 kW.

For example, the NVIDIA H100 GPU has a peak power consumption of 700 W. This is 1 hp of power consumption for one AI processor module. If the rail voltage rail is 1.8 V, this is a current draw of 400 A.

This is roughly equivalent to what an internal combustion car's starter motor draws, which is why battery jumper cables are so thick. A Tesla electric motor only draws 200 A when it is accelerating. Other processor chips are in the same category, drawing 500 to 1000 A, but at lower rail voltages.

The estimated sales volume of the H100 in 2024 is about 2 million units, or about 3.5 million units cumulatively since it was introduced. When all of these processors are operating, the

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processors alone will consume 2.5 GW of power, not including the rest of the electronics and their cooling systems. A U.S. household uses about 1 kW of power on average. This is equivalent to the power consumption of 2.5 million households, or the entirety of Los Angeles.

According to the International Energy Agency, in 2022, data centers worldwide consumed a total of 460 Twatt-hours of energy, accounting for 2% of global electricity usage. This is, on average, 40 GW of electric power usage. In the U.S., data centers accounted for about 6% of total power consumption. In Ireland, data centers accounted for 17% of the nation's power usage in 2022. Power usage in data centers is expected to almost double by 2025. This means data centers could account for nearly 10% of the U.S. power consumption within the next few years.

According to the Newmark study, "Energy is the number one challenge for the data center market." It is no wonder that Microsoft, Google, and Amazon have struck deals with operators and developers of nuclear power plants, according to the *New York Times*. Microsoft was reported to have made a deal to revive the Three Mile Island nuclear plant in Pennsylvania. Amazon and Google have stated that they are considering new, modular nuclear plants, located adjacent to their data centers. Okla, a developer of modular nuclear power plants, signed a 20-year purchase agreement with Wyoming Hyperscale to use Okla's Aurora powerhouse to power new data center campuses.

Just as important to adding to the power grid is reducing the demand for power by more efficient chip design and power delivery. For a 1000 A processor operating at 1 V, the resistive load created by the chip is 1 mΩ. For the IR losses to be less than 10% of the power consumption, the DC resistance in the power distribution path needs to be less than 100 μΩ. This means more and thicker copper layers and optimal design of the via field from the copper layers to the device being powered. This means measurement capability in the μΩ range to test the final designs.

The Industrial Revolution began with harnessing power sources that amplified the ability of a person. With today's generation of AI and network processors, one single chip requires 1 hp to operate. The need for speed will be the driving force behind energy production and efforts to make increasingly efficient use of available energy.

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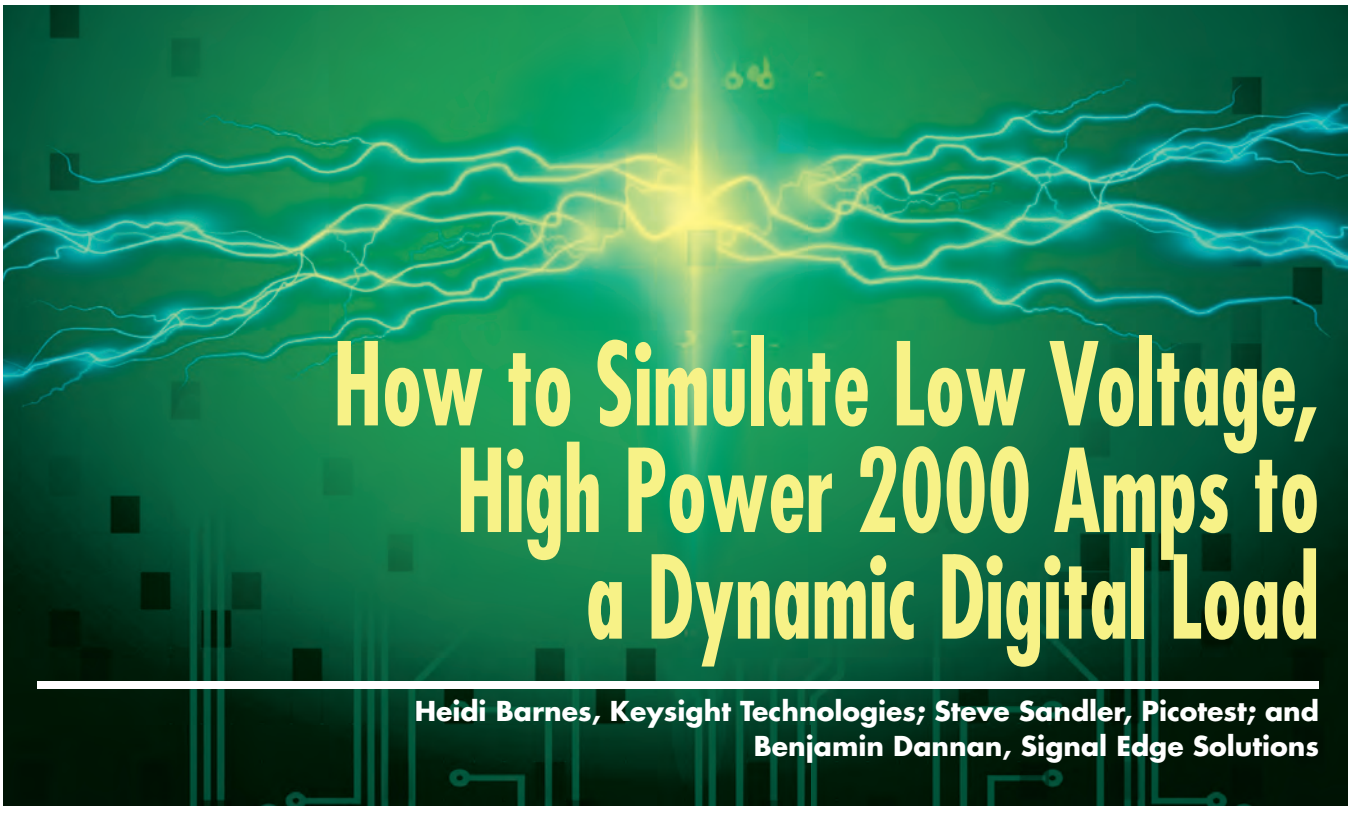
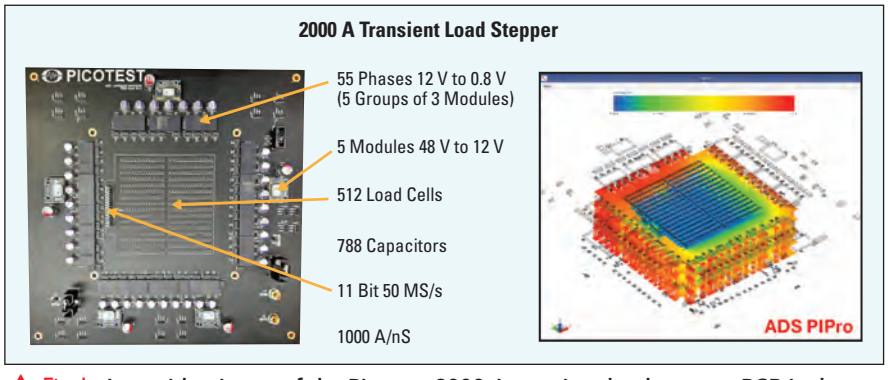


How to Simulate Low Voltage, High Power 2000 Amps to a Dynamic Digital Load

Heidi Barnes, Keysight Technologies; Steve Sandler, Picotest; and Benjamin Dannan, Signal Edge Solutions

Hardware engineers are learning the hard way that power integrity (PI) requires electromagnetic (EM) simulation of the printed circuit board (PCB) power delivery network (PDN). Traditional rules-of-thumb and leveraging data sheet examples are not an option as designs move from hundreds of Amps (A) to thousands. 1000 A across a 100 microhm (μΩ) PCB PDN is still 100 millivolts (mV) of IR drop and 100 Watts (W) of power dissipating as heat. This is one of the fundamental reasons for transporting power at a higher voltage and lower current for as far as possible. Less power lost in the path to the load. The other reason is impedance. Power rail voltage ripple is a direct result of dynamic di/dt currents interacting with the path impedance. When currents go up, the target impedance must go down to keep power rail voltage ripple within specified limits. Controlling the power delivery DC resistance and the parasitic path inductances of the PCB is a critical part of creating a Digital Twin model for designing a 2000 A PDN for a dynamic digital load.

Figure 1 shows an example of a 2000 A PDN design that Picotest uses to demonstrate their 2000 A 11-bit programmable transient load stepper.[1] This design was imported into a 3D-EM simulator to validate DC, electrothermal, and AC impedance design performance.



▲ Fig. 1 **A topside picture of the Picotest 2000 A transient load stepper PCB is shown on the left. The PCB CAD data is imported into a full 3D-EM simulator to validate DC, electrothermal, and AC impedance performance.**

WHAT IS DRIVING THE NEED FOR A PCB PDN EM MODEL?

To explain why the impedance of a 2000 A PDN is orders of magnitude harder than expected, one can combine the traditional target impedance equation with the need to minimize power. The PI engineer defines a target impedance so that a di/dt at any frequency, DC to GHz, will not result in exceeding the maximum allowed voltage ripple. The equation for target impedance is simply the maximum delta allowed voltage ripple divided by

the worst case dynamic delta current change, as shown in Equation 1.

$$Z_{Target} = \frac{\Delta V_{Max\ Ripple}}{\Delta I_{Max\ Transient\ Load}} \quad (1)$$

Combining this equation with the maximum available power provides an interesting look at the challenge PI engineers are facing. The relation between power and current can be estimated by the ideal DC-DC converter equation, where power in equals the power out, as shown in Equation 2:

$$P = V_{in} \times I_{in} = DV_{in} \times \frac{1}{D} I_{in} \quad (2)$$

where D is the duty cycle of the DC-DC regulator.

Here, D is less than or equal to 1, and shows how the current can be proportionally increased as the voltage is decreased with a point-of-load DC-DC converter while maintaining the same power level. If the allowed voltage ripple is set to 5% and the maximum delta current transient to 50% of the maximum current, then Equation 3 can estimate Z_{Target} as a function of voltage for a set power level:

$$Z_{Target} = \frac{D \times V_{in} \times 5\%}{\frac{1}{D} \times I_{in\_max} \times 50\%}$$

$$= D^2 \frac{V_{in}}{I_{in\_max}} \times 10\%$$

$$= \frac{(D \times V_{in})^2}{P_{max}} \times 10\% \quad (3)$$

Plotting Z_{Target} as a function of the DC/DC converter output voltage, $D \times V_{in}$, while holding the power constant for a given application shows an exponential decrease in target impedance, shown in ***Figure 2***. A USB design at 4.5 W and 5 Volts (V) has a target design impedance in the hundreds of milliohms (mΩ) and may not be impacted by PCB PDN path parasitics; however, if the voltage is dropped down to sub-1 V levels, then Z_{Target} can easily drop into tens of mΩ. Typical FPGA designs at around 34 W with a 12 V input power connector to the PCB quickly drop to a Z_{Target} of a few mΩ for the sub 1 V core power rail. Finally, for the new generation of AI and cloud compute chips running at 1600 W, the target impedance at 12 V is already a challenge at 1 mΩ levels. This helps to explain why 48 V power rails and higher are now showing up in electronic designs to reduce the impact of PCB path parasitics until the final point-of-load DC-DC conversion, where the 2000 A is needed. Running 1600 W on a sub-1 V power rail drops the design target impedance into the tens of μΩ.

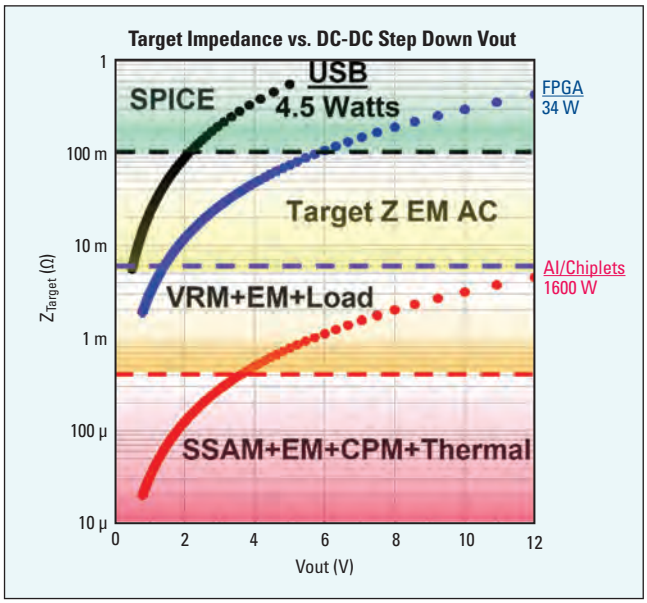


Fig. 2 **A plot showing how target impedance decreases with the output voltage of a DC-DC regulator for a given application where the power is held constant. As the output voltage drops the current increases proportionally, but the target impedance decreases exponentially.**

Historically, SPICE simulations without PCB EM models have been used for designs above 100 mΩ. The concept of Z_{Target} and the need to include the PCB parasitics as an EM model became necessary as target impedances decreased to tens of mΩ. A typical PCB PDN with 5 cm between the voltage regulator module (VRM) and the load can easily have mΩ of DC path resistance and hundreds of pHs of inductance that can no longer be considered small in proportion to Z_{Target}. As Z_{Target} decreases from mΩ to μΩ, there is also an increasing demand for higher fidelity Digital Twin PDN simulations that include VRM behavioral models and worst case dynamic loads.[2]

HOW TO CREATE THE PCB PDN EM MODEL

Knowing that PCB EM parasitics are a critical part of designing a 2000 A power delivery network, the next question is how to create and use a PCB PDN EM model in a simulation. EM simulator tools like Keysight's ADS with PIPro EM are optimized for multi-layer laminate PCB PDN simulations. The designs are imported from fabrication files like ODB++™ and IPC-2581™ with access to components, net names, and PCB stackups that allow for an increased level of automation when setting up a full 3D-EM analysis. EM models are needed for DC IR drop, DC Electrothermal, and AC impedance. DC IR drop models can quickly identify any asymmetries in the voltage delivery to large digital loads with hundreds of power and ground pins. Optimum locations for sense lines can be found, and layouts modified to maximize the uniformity of the power delivery. DC electrothermal simulations can help determine the amount of cooling required and the trade-offs between thicker copper layers versus adding more layers to prevent thermal run away and improve reliability (see ***Figure 3***).[1]

AC Impedance EM models are a critical part

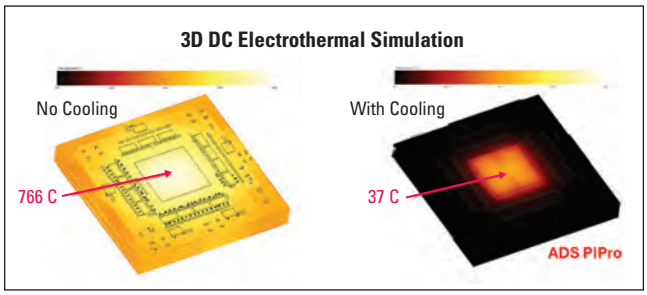


Fig. 3 DC electrothermal simulation of the Picotest 2000 A transient load stepper showing the importance of water cooling to prevent thermal runaway.

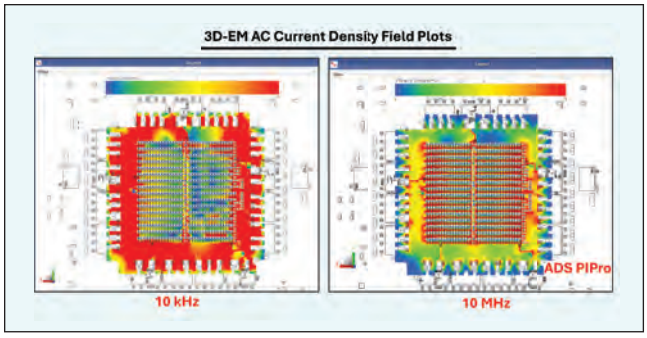


Fig. 4 The 3D EM AC current density plots for the Picotest 2000 A transient load stepper show how the current delivery changes from the VRMs at 10 kHz to the decoupling capacitors under the load cells at 10 MHz.

of the Digital Twin PDN model that can simulate transient behavior to validate the pass/fail ripple voltages on the power rail. The PCB AC Impedance EM model can also be used to look at the spatial distribution of current densities over frequencies. The current density plots in ***Figure 4*** show how the VRMs deliver power from the edges at low frequency, while the decoupling capacitors under the 512 load cells dominate at 10 MHz.

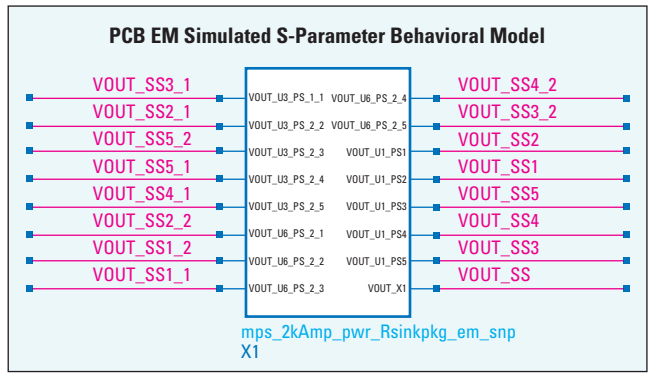


Fig. 5 The PCB PDN EM model can be exported as an S-parameter behavioral model.

The AC impedance model includes ports for the decoupling capacitors so values can be optimized to meet a desired Z_{Target} in the frequency domain. This decoupling capacitor optimization is best done before adding the EM model to the end-to-end PI Digital Twin simulation. To use the AC Impedance EM model in a PI Digital Twin simulation, it can be saved as an S-parameter behavioral model, as shown in ***Figure 5***, with connecting ports to the VRM, the load, and passive components, such as decoupling capacitors.[1]

HOW TO CREATE THE SWITCHING VRM MODEL AND TRANSIENT LOAD

The PI Digital Twin connection to the VRM needs to be a behavioral model of the VRM that can handle the large signal dynamic behavior of the DC-DC converter's interaction with the load. Complete transistor level models of a VRM may work for evaluating set point characteristics, but when connected to real-world PCB EM models and dynamic loads, a transistor level simulation can fail to converge or

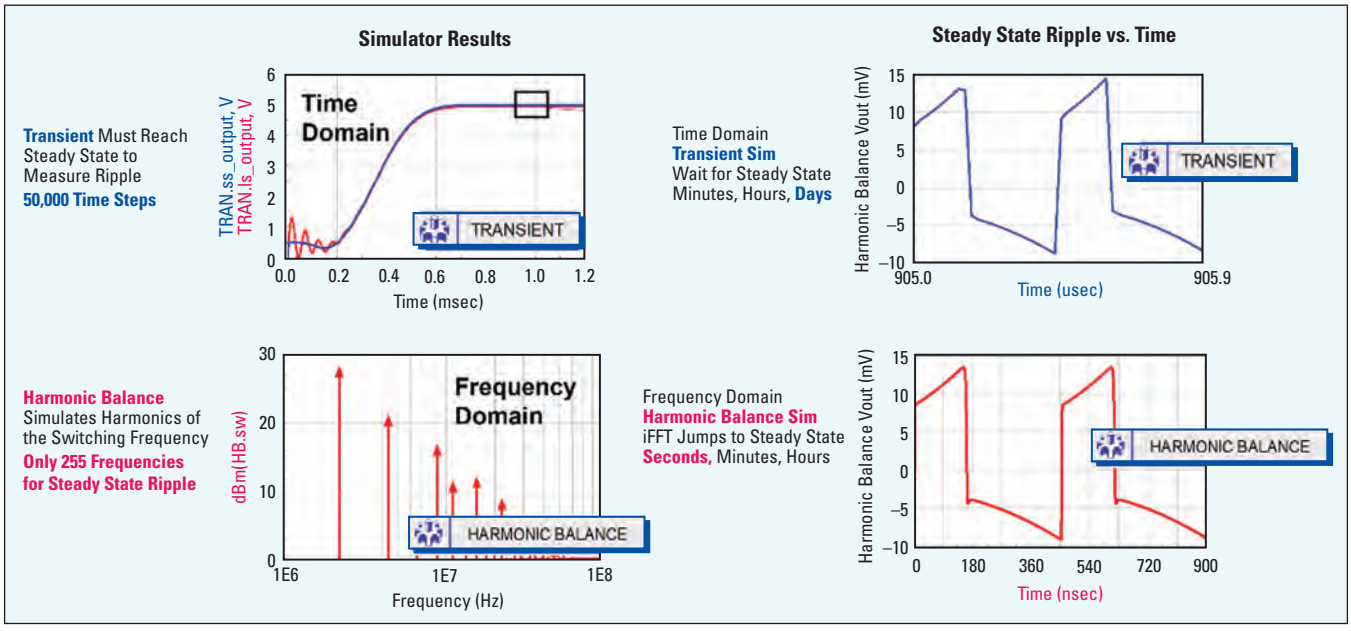


Fig. 6 The plots on the top show how a transient simulator must wait to reach steady state before the voltage ripple can be measured, while the bottom plots show how HB can simulate enough harmonics of the switching frequency to directly convert to the steady state voltage ripple solution.

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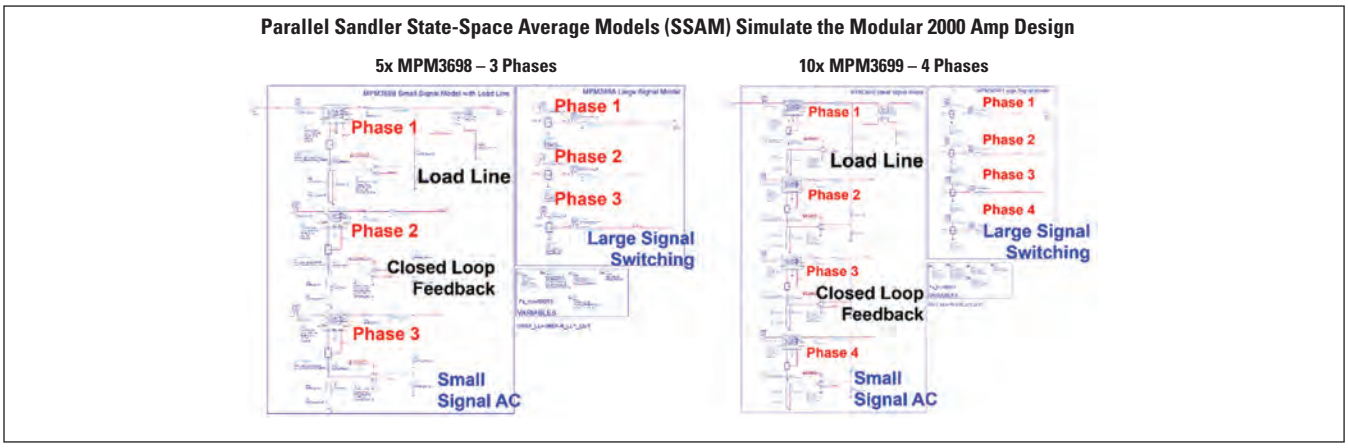
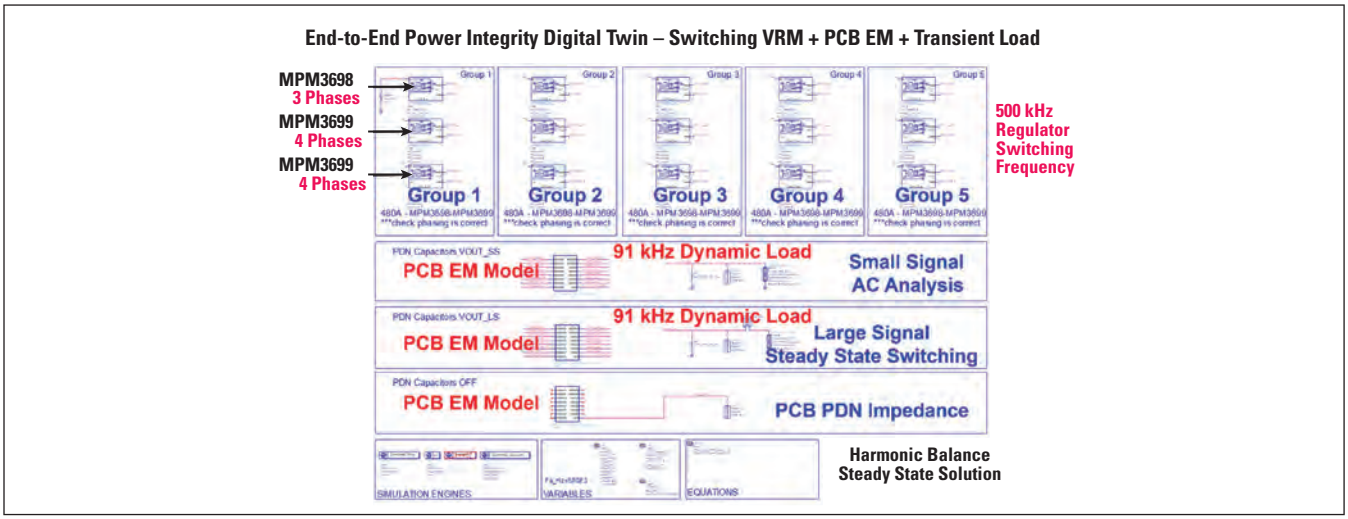


▲ Fig. 7 The modular design of the off-the-shelf VRMs allows paralleling the output phase to get to 2000 A. In simulation, all the phases are using the same VRM SSAM model.



▲ Fig. 8 The end-to-end PI PDN Digital Twin with 55 VRM phases switching at 500 kHz, connected to a PCB PDN EM model, and a transient 91 kHz switching load. The circuit uses an S-parameter simulator for PDN impedances and HB for steady state large signal transient ripple.

take days to run. To get around this problem, the Sandler state-space-average (SSAM) VRM behavioral model can be used.[3] This model captures the classic behavior of a switched mode power supply design including the feedback characteristics to create both small signal AC behavior and large signal switching transients. The reason for this type of behavioral model is that it can be run both in a traditional transient SPICE simulation, or in the frequency domain using harmonic balance (HB). HB is a powerful technique that simulates a circuit with enough harmonics of the fundamental frequency to convert the spectral data to the time domain using an iFFT. The benefit is that the HB simulation jumps directly to the steady state condition and avoids the longer simulation times required for a transient simulation to reach steady state. Running the switching model in both a transient SPICE simulator and the HB simulator shows that they get the same result (see ***Figure 6***).[4]

This SSAM VRM model can easily be paralleled together to represent the 55 phases of the VRMs each delivering ~36 A to reach a total of 2000 A for the Picotest 2000 A transient load stepper design (see ***Figure 7***).

The last step in creating the Digital Twin is to add the behavior of the load. This can include the passive S-parameter behavioral model of the package die PDN and a dynamic current I(t) of the load. Here, a switch model that can run in transient or HB is once again used to create a switching transient load at the desired frequency.[1]

THE COMPLETE PI PDN DIGITAL TWIN

The complete 2000 A PI Digital Twin model is shown in ***Figure 8***. The PCB EM model connected to the dynamic load is replicated twice; one is connected to the small signal AC output from the SSAM, and the other is connected to the SSAM large signal switching output. A third path with just the PCB EM model is also added to provide impedance information.

Simulating just the impedance helps to identify resonances with higher impedance that can lead to worst case power rail ripple if excited with a dynamic load. In this design, there is a peak in the

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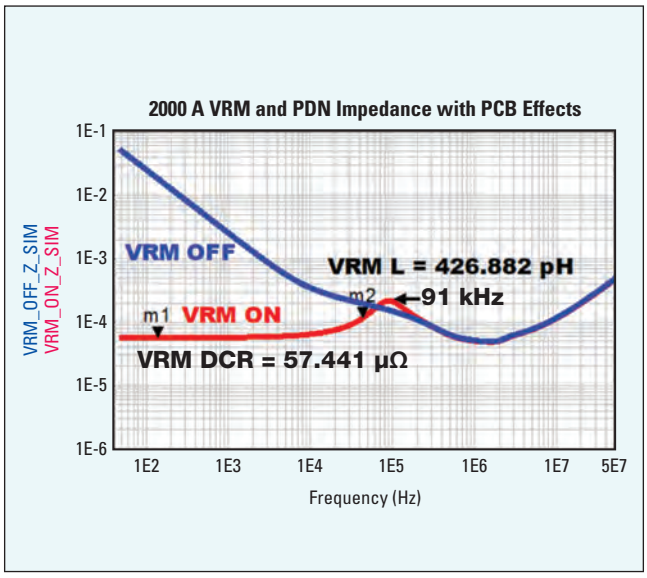

Fig. 9 **Simulating the PI Digital Twin in the frequency domain with the VRM on and off shows how the VRM controls the impedance below 30 MHz, and at 91 kHz there is an impedance peak indicating a resonance in the PDN.**

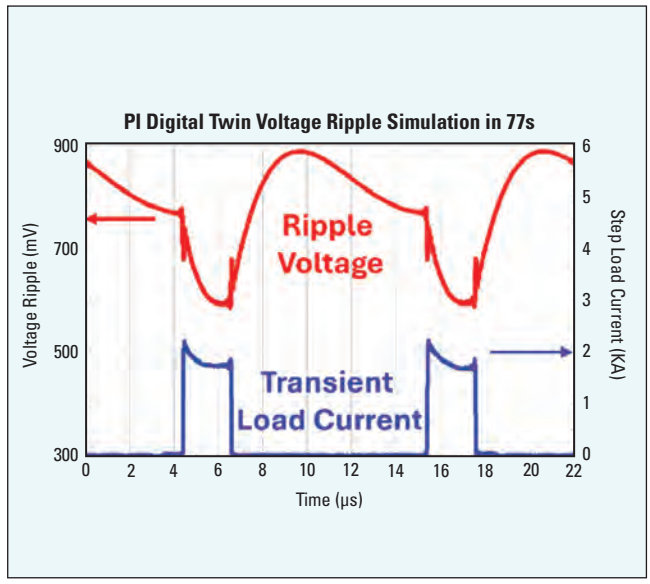

Fig. 10 **The PI PDN Digital Twin simulates in 77s with all 55 phases of the VRMs switching at 500 kHz and the 2000 A transient load switching at 91 kHz.**

impedance around 91 kHz (see ***Figure 9***). This resonance is a result of higher than desired output impedance from the VRMs, and a limited amount of bulk capacitance. The desire was to push the performance of the VRM technology instead of spending more money and space for the bulk capacitors in this initial demonstration of the Picotest 2000 A transient load stepper.[1]

Knowing that a dynamic load switching at 91 kHz can excite this resonance and cause a worst case voltage ripple, the 2000 A PDN Digital Twin is then run with this worst case 2000 A load being turned on and off at 91 kHz.[2] The 55 phases of the VRMs are all switching at 500 kHz with different phases to deliver the dynamic 2000 A current to the 91 kHz load. The HB simulator runs this full PI Digital Twin simulation in less than 77 seconds (see ***Figure 10***).

The PI Digital Twin shows the corresponding undershoot (droop) and overshoot (kick) that occurs with the 2000 A load. Making design modifications with the PI Digital Twin that simulates in 77 seconds can build engineering intuition, save hours of engineering debug time on the bench, and mitigate expensive hardware failures.

CONCLUSION

Including the EM behavioral model of the PCB PDN parasitics is now a critical part of designing and validating a 2000 A PDN. The orders of magnitude drop in Z_{Target} from hundreds of mΩ to tens of µΩ is driving the need for higher fidelity PI PDN Digital Twin simulations that include a dynamic switching VRM model, the PCB PDN EM model, and a worst case transient load model to validate the design before fabrication. Behavioral VRM models like the Sandler SSAM and transient load switch models that run in HB have a significant simulation time savings advantage by jumping directly to the steady state results for fast optimization and debugging of a design. Digital Twin HB simulations can run in a matter of seconds or minutes compared to transient simulations, which can take hours or even days when including the PCB EM model. Creating the PCB PDN EM model also continues to get easier. EM simulators that are optimized for PCB PDN simulations provide an increased level of automation to enable the basics of DC IR Drop, electrothermal, and AC impedance for early detection of design issues. The ability to optimize a PDN for Z_{Target} with PCB parasitics in the frequency domain and to then export to an end-to-end PI Digital Twin simulation for validation in the time domain should be standard practice for the PI engineer.

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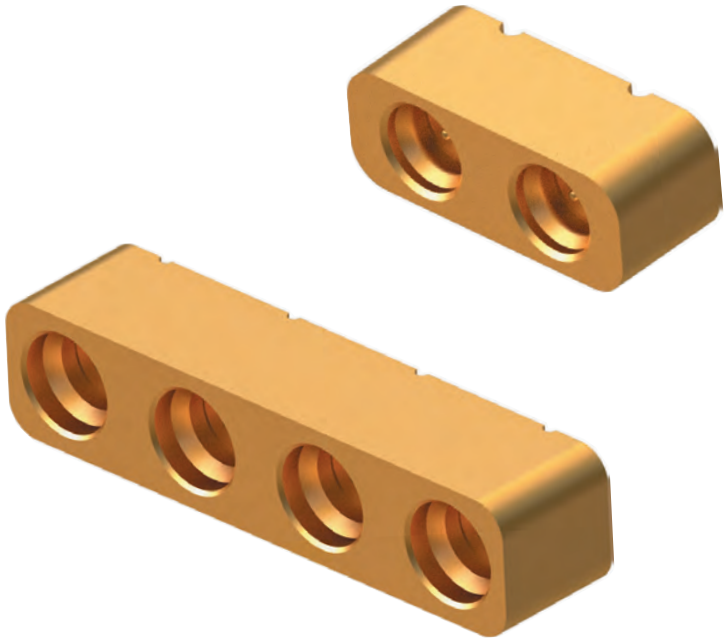

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Reflections on the Origins of COM

Rich Mellitz, Samtec

Channel operating margin (COM) is a well-documented IEEE standard that has been used successfully since 2014 in the design of channels and specification of interconnect. The goal of this article is not to explain what COM is, or how it works (see the reference section for this information). Rather, this article reflects on the COM origin story as recalled by Rich Mellitz, who was in the room when the need for something like COM was realized, and who was one of the chief architects of the spec. The following aims to capture the story of the creation of the COM standard in the words of Mellitz, as well as its evolution and where it might be headed next.

Some would argue that it all began in the 1990s with the needs of PCI Express®, InfiniBand™, 10 Gbps Ethernet,[1] and when semiconductor companies had to specify electrical channels. These electrical channels use separate differential pairs for transmit and receive. Here, the term "line" is intended to mean one transmit to receive differential pair.

Before getting too far into the story of COM, it might be best to also define what is meant by data rate. IEEE specifies the delivered data rate for a MAC. For example, 10 Gbps Ethernet[1] was really 10 Gbps Ethernet on four pairs of twinaxial cabling. In other words, 2.5 Gbps per line. However, since the data was 8B10B NRZ encoded, the actual line rate was 3.125 Gbps. Thus, the Nyquist rate is 1.5625 GHz. This is different from PCIe, OIF, and InfiniBand, where the data rate is actual symbol transfer rate per line. For convenience, one can simply refer to 25 Gbps, 50 Gbps, 100 Gbps, 200 Gbps, and 400 Gbps per line without detailing the actual data rate load for encoding.

Identifying the Problem (1990-2010)

In the 1990s, copper electrical bus rates were mostly under a gigahertz. Losses and crosstalk below a gigahertz are generally considered "well behaved" because the electrical wavelengths are on the order of PCB design sizes. At this time, it was sufficient for many semiconductor manufacturers to have rudimentary channel requirements based on characteristics described as simple functions of frequency. Eye diagrams emerged for compliance testing, augmenting the typical test method of the time: set up and hold timing verification.

Around 2002, IEEE's Ethernet broke the 10 Gbps barrier, which led to other 10 Gbps projects, such as IEEE Std 802.3ap-2007[2], where 10 Gbps per line interconnect channels were defined for a backplane and data center twinaxial cabling. The focus for the 10 Gbps copper backplane and cable project was frequency domain (FD) limit masks to support a 1-m backplane reach objective. Although this was sufficient for interconnect designers of the time, unfortunately, the interaction between these masks and transceiver specifications was somewhat weak.

In 2010, the IEEE project IEEE Std 802.3ba-2010[3] extended inter-box cabling to 7 m of electrical cable using the same 10 Gbps FD masks for electrical channel compliance. 2012

showed a push for 25 Gbps per line as the IEEE 100 Gbps Backplane and Copper Study Group[4] kicked off. Electrical lengths of concern shrank to about an inch as a result of the 25 Gbps per line signaling. This broke the FD mask paradigm because in order to make channel compliance work, too much guard band would be needed. Essentially, there was no easy way to budget between insertion loss, crosstalk, return loss, and transceiver capability. This need paved the way for COM.

Very quickly, it was discovered that relying on maximum insertion loss was not sufficient. It was also realized that insertion loss curves near 13 GHz were not smooth. The aberrations around a fitted, smooth, insertion loss curve were called insertion loss deviation (ILD). More ILD meant less margin. What caused this was that via/connector/package geometries and the spacing between them were approaching the critical electrical lengths. This resulted in reflection starting at 5 GHz. It was known that more reflection caused more ripple in the insertion loss curve, and semiconductor manufacturers indicated this would result in lower performance. The frequencies of interconnect impairments also spawned conversation contrasting NRZ and PAM4. Although NRZ dominated 25 Gbps designs, the 50 Gbps line rate favored PAM4.

Crosstalk was another issue addressed during the 10 Gbps per line project.[2] Crosstalk was converted to a single RMS voltage, called integrated crosstalk noise (ICN), which is computed with the normalized integration of the power sum of all frequencies in the crosstalk responses. (Recall Parseval's theorem, which states that total power in the time domain is the same as total power in the FD.) In addition, insertion loss to crosstalk ratio (ICR) was borrowed from J. Salz's work,[5] supporting the notion of a budget between crosstalk and insertion loss.

At around the same time, some people were having discussions about how to determine a maximum channel capability based upon the Salz limit.[5] This tactic had been used for the higher power, lower radix "BaseT" standards. The assumption is that transceivers have at their disposal unlimited DFE and FFE. Data center switch and network cards require orders of magnitude less power per line and have an order of magnitude higher radix and density. The Salz limit was interesting, but required too much power for the backplane application. So, the industry ended up focusing on ILD and ICR, as these were the things that were important for physical design.

In 2010, there was still no standard method or simulation to evaluate performance. Specifically, there was a lack of signal integrity simulation standardization. The result was that standards development was relegated to what could be called the "ouch test." The interconnect designers would create BGA ball to BGA ball models called channels, and transceiver vendors would say "ouch" when the channel was too tough or not working in a lab experiment. For standards development, deciding on channel and transceiver parameters was kind of like playing poker. Unfortunately, at the time, there was a significant disconnect between physical design and what the simulations could provide.

During this time, interconnect designers seemed happy using insertion loss, return loss, crosstalk, and ICR curves, gaining apparent performance by minimizing ICN and ILD for design. Unfortunately, the FD bounds, while good for interconnect designers, were of limited use for transceiver designers. Consider that the 10 Gbps backplane ILD mask was reasonable for the physical design of data center switches and servers. The original expectation was that five DFE taps would handle the data center designs like IBM's Blade Center. The disconnect was that the actual designs requited up to 50 DFE taps. Moving to 25 Gbps per lane (25G), it was realized that a linkage was needed between the physical channel design and transceiver or SerDes design. The two spoke different languages. This growing need for a "Rosetta Stone" paved the way for something like COM.

COM Evolution (2011-Present)

Interconnect designers require a budget that includes insertion loss, crosstalk, and reflections. However, consideration of SerDes needs must also be part of this budget. Around 2010-2011, the group was working on projects for 25G and started to experiment with post processed FD metrics graduating to including a "dibit" time domain response suggested by Charles Moore.[6] The method was mostly based on power losses, but did not have direct linkage to the time sampled SerDes. This opened the door to time domain.

Early in the 25G project, the group started examining the channel pulse response. A data stream is made up of a pulse response convolved with a symbol stream. A pulse response was recognized as perhaps the lynchpin that would connect the SerDes designer and interconnect designer. Many published works suggested that a SerDes architect could translate pulse responses into design capability. Anecdotally, interconnect designers can see direct effects of features that resulted from loss, reflection, and crosstalk.

Prior to the COM proposal, there was a lot of angst about converting S-parameter measurements made in the FD into a pulse response in the time domain. Determining a pulse response is somewhat easier if a transmitter filter, receiver filter, and a pulse response filter are applied before converting the S-parameter into a pulse response using an FFT.

At that time, SiSoft (now part of MathWorks) had a proprietary way to create a pulse response from FD S-parameters, and SiSoft employees were active in the IEEE meetings. Walter Katz (SiSoft) favorably correlated pulse responses, which they compared to the pulse responses for a filtered FFT method were considered for COM.[7] This is when things started to get interesting. The turning point was moving discussions to pulse response analysis.

Pulse responses sampled at one symbol interval correlate to one unit interval (UI) spaced samples in a data stream waveform (because of linear time invariance and convolution). For these purposes, UI corresponded to the time between symbol samples. The RMS of the data waveform sampled at one UI represents voltage average power. The same voltage average power could be determined by taking the root of sum of the squares (RSS) of the samples in the pulse (as long as the data was somewhat random). An inter-symbol interference (ISI) noise vector was created by not including the sample at the pulse peak. Since crosstalk is all noise, the entire sampled crosstalk pulse response was used as noise. There was now a way to combine crosstalk with reflections, and then compare them to pulse peak (which would be proportional to insertion loss).

Next, the group began to discuss cursors, which refer to samples of the victim response space at one UI. The peak sample index is cursor 0. Samples before would be negative cursors and samples after would be positive cursors.

The industry needed to move to the statistical domain. The RSS for samples of a pulse response is ISI. It corresponds to the RMS of respective sampled noise of the random data response. RMS noise can be considered a normal or Gaussian distribution. Enter the statistics of noise. The group talked about voltage of noise at certain probability, such as a probability of 1e-12 corresponds to ± 7 sigma where sigma is the RMS. Much discussion ensued about whether the assumption of Gaussian noise was overly pessimistic for copper channels.

During the same era, other standard groups addressed the issues of expected noise. Work on PCI Express Generation 1 and 2 and SAS/SATA, for example, centered around data patterns that created the worst-case ISI or noise. This concept was called peak distortion. The objective in the IEEE project was to address the ISI that corresponded to a line error rate of close to 1e-12. The worst-case ISI error rate is typically many orders of magnitude lower. Conversations started by aligning samples to the pulse peak. The group addressed actual clock and data recovery sampling much later. The sum of the magnitude of the 40 worst UI spaced samples in the pulse response would seem to correspond to probability of 1e-12.

What was significant here was the whole notion of doing statistical analysis with crosstalk. What are the statistics that should be used? Should the industry just use RMS values for everything? One of the discoveries during this process was that, when using statistical Gaussian noise assumptions for the noise one gets in backplanes and cables, one ends up completely over designing.[8] In other words, one overpredicts the noise by quite a bit as required by a maximum bit error ratio. That did not sit well, so the group decided to use what was considered to be the "real" noise profiles that are generated. This was the point when COM could take advantage of the actual nature of electrical channels. Actual electrical crosstalk and ISI noise distributions were not independent and identically distributed (IID) random processes.

Then, a curious thing happened. People started publishing their interconnect models. The IEEE working groups became a public repository for channel models that were representative of interconnects being produced, including backplanes and cables. In the past, someone might show you a picture and graphs of their interconnect. But once 25 Gbps was reached, everyone realized it was a way to manage the standard process by using channel S-parameter models of what the industry might be doing or planning. This became even more prolific at 50 Gbps. These models are a management tool for standards development. The other half is managing transmit and receive parameters, which were embodied as COM parameter tables to be incorporated into the standard.

COM was proposed in 2012 for a channel compliance method[9], which included the IID nature of interconnect and minimum transceiver capability. Transceiver capability is embodied in the tables within the standard. COM is a documented algorithm in IEEE802.3 and it is NRZ and PAM4 capable. An evolutionary MATLAB example script was used throughout all the projects which used COM (see ***Figure 1***). Although not a standard compliance, the script proved useful to move the wave of standards development.

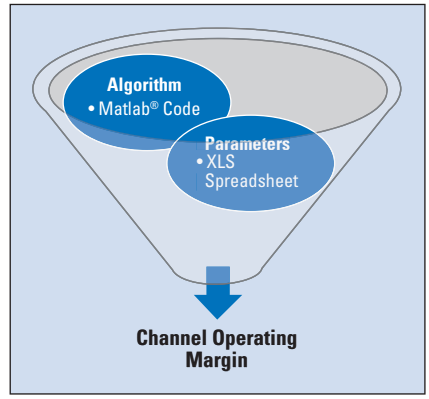

Fig. 1 Implementation of COM.

Parameters are represented in a spreadsheet which the MATLAB script uses to statistically evaluate electrical S-parameter channel models using an algorithm procedure described in Annex 93A and presently for 200 Gbps An-

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nex 178A of the IEEE 802.3 Ethernet standards. Moving forward, there are plans to incorporate the MATLAB COM script and associated spreadsheets in an IEEE SA Open Source under an IEEE802.3 umbrella, which will lead to a new COM evolution.

Since its inception as part of the 802.3bj project, COM has undergone many revisions based upon industry needs and changing market potential. It has been adopted for other IEEE projects such as IEEE Std 802.3bm-2015,[10] IEEE Std 802.3by-2016,[11] IEEE Std 802.3bs-2017,[12] IEEE Std 802.3cd-2018,[13] IEEE Std 802.3ck-2022,[14] IEEE Std 802.3df-2024,[15] and IEEE P802.3dj.[16] In addition, COM has been borrowed for OIF and InfiniBand standards, which dovetail with IEEE standards.

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Richard Mellitz *is presently a Distinguished Engineer at Samtec, supporting interconnect signal integrity and industry standards. Richard has been a key contributor to IEEE802.3 electrical standards for many years. He led efforts to develop radically new IEEE and OIF time domain specification methods called COM and Effective Return Loss. Early in his career, he founded and chaired an IPC committee authoring the industry's first TDR standard. Richard holds many patents in interconnect, signal integrity, design, and test. Richard received the IEEE Standards Association Medallion and the Intel Achievement Award for spearheading the industry's first graduate signal integrity programs at the University of South Carolina. Richard was also honored with the DesignCon 2022 Engineer of the Year Award.*

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"How to Measure Ultra-Low Impedance (100uOhm and Lower) PDNs" was presented at EDI CON University in 2018. The presentation concluded with the mathematical relationships in ultra-low impedance measurements, determining the major obstacles and the mathematical solutions.

$$V_{measured} = 0.223 \cdot \sqrt{e^{0.2306 \cdot dBm}} \cdot \left[\frac{DUT}{DUT + \frac{R_{port}}{2}} + \frac{1}{CMRR} \cdot \frac{R_{\_shield\_1}}{R_{\_shield\_1} + R_{port}} + \frac{1}{10^{\frac{Noise\_Floor}{20}}} \right] + \underbrace{PDN\_V_{noise}}_{\text{Error (Noise)}} \quad (1)$$

The increased core current for the latest AI, data center, and super computing segments made this measurement a lot more complicated, with power distribution network (PDN) impedance now as low as 10 μΩ. Performing this measurement is a challenge, but it is far more difficult than simply performing the measurement. Many, if not most, new boards are liquid-cooled. While some are just refrigerated liquid, others are refrigerated and immersion cooled. Setting up this cooling is not trivial, and some joke that as a power integrity engineer in today's environment, one needs to be educated in plumbing. Due to this complexity, it would be much more desirable to perform the measurement without cooling, requiring that the measurement be performed very quickly.

There is an additional challenge: while many are accustomed to measuring small signal impedance with a vector network analyzer (VNA), at these higher currents, there are large signal effects. The impedance is not constant but has a nonlinear load dependency. This is evident in the step load test results shown in ***Figure 1***. The load is stepped from 1500 to 750 A and then from 750 to 0 A. Despite the current change being 750 A in both cases, the voltage excursions are notably different, both in response amplitude and in recovery time.

Therefore, three challenges are presented: how to measure either the small signal response or the large signal response; how to do so extremely quickly so it does not overheat without the attached cooling system; and how to do so for a 10 μΩ active PDN. This article will provide a few viable options, each of which can be performed using the same equipment.

The path here is to use a sophisticated and novel Fast Fourier Transform (FFT) based 3-port measurement (V/I). This method involves applying digitally modulated patterns to create modulated load currents up to 1500 A and recording the resulting power rail voltage perturbations.

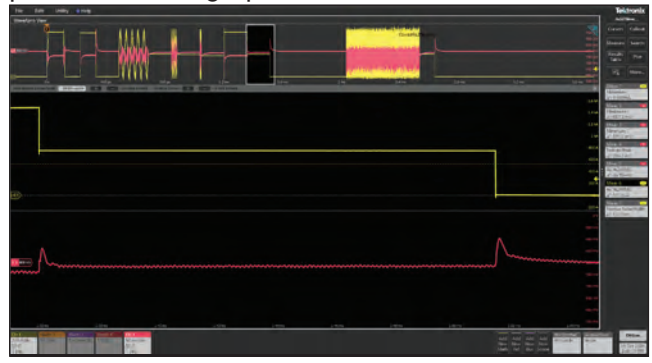

Fig. 1 The load is stepped from 1500 to 750 A and then from 750 to 0 A; note the asymmetrical responses. Other more complex step load patterns can be discerned in the upper gray areas.

(Re)Establishing the Issues

The final equation in the university paper referenced previously provided the mathematical description of the measurement and the limitations. This compact equation showed that the low frequency ground loop error is the result of the cable shield resistance and the isolator Common Mode Rejection Ratio (CMRR). The equation also included external PDN noise and the measurement noise floor. The theory is proven at the end of this presentation with the measurement of a 20 µΩ resistor.

Despite the appearance that a solution already exists, there are a few shortcomings, one being that this measurement is of a passive resistor. Active power supplies are not quiet; in fact, they can be quite noisy. Equation 1 included noise as a term that has been ignored thus far. The equation indicates requirements of 10 µΩ, so for the future, one needs a plan for measuring well below that.

Using Equation 1, the CMRR required for the measurement is solved as a percent error. In the case of a probe, the ground pin resistance is added to the shield ground in the numerator. The device under test (DUT) magnitude and percent error are in the denominator. Together, these establish the required CMRR.

$$CMRR = 20 \cdot \log\left[\frac{Rcable + Rpin}{DUT \cdot Error\%}\right] \quad (2)$$

The P2102A 2-port probe from the article is then used as an example to measure a 10 µΩ DUT with an uncorrected error of 10%:

$$CMRR = 20 \cdot \log\left[\frac{30\ m\Omega}{10\ \mu\Omega \cdot 10\%}\right] = 89.5\ dB \quad (3)$$

This is within the CMRR of the J2114A isolator shown in the article, so theoretically this measurement can be accomplished. However, at this point, one encounters the limitations caused by the power supply noise.

With the caveat that all power rails and voltage regulator models (Vrms) are different, and Constant-On-Time (COT and all derivatives) are noisier than pulse width modulation (PWM) Vrms, ***Figure 2*** shows the power rail noise of the 1500 A ICONIC demo board (PWM).

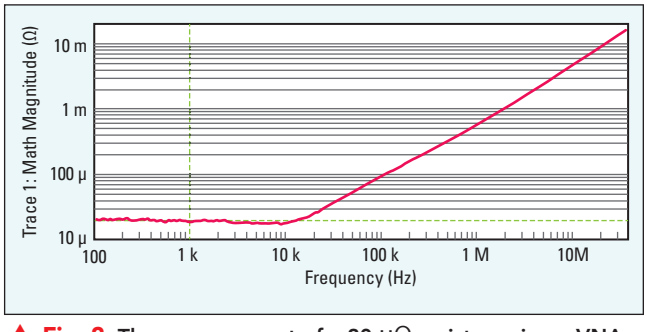

Fig. 2 The measurement of a 20 µΩ resistor using a VNA in the 2-port shunt-through configuration.

Figure 3 shows the noise density to be in the range of -80 dBm. Using the 2-port shunt-through impedance measurement configuration, the attenuation of the signal, S21, is expressed as:

$$S21 = \frac{DUT}{DUT + 25} \quad (4)$$

At 10 µΩ, this is

$$S21 = 20 \cdot log\left[\frac{10\ u\Omega}{10\ \mu\Omega \cdot 25\ \Omega}\right] = -128\ dB \quad (5)$$

This establishes the source power required for the measurement. Using the noise floor of -80 dBm and the signal attenuation of 128 dB:

$$Source_{\_dBm} = noise\_floor + S21 \text{ and } Source_{dBm} = -80\ dBm + 128\ dB = 48\ dBm \quad (6)$$

To be fair, the signal-to-noise ratio (SNR) requires the signal to be at least 6 to 10 dB above this for a decent measurement. Therefore, the minimum will be set at 54 dBm.

Using the Bode 100 VNA (which has a relatively high source power of +13 dBm) in combination with the B-AMP 12 amplifier adds 12 dB gain, resulting in 25 dBm, almost 30 dB short.

How much is 54 dBm?

$$Vrms(dBm) = 0.223 \cdot e^{0.23026 \cdot dBm} \quad (7)$$

This requires a 110 Vrms source signal to overcome the noise. Alternatively, the power plane noise of -80 dBm is 22 µVrms. A minimum 6 dB SNR requires a minimum of 44 µVrms to be applied to the DUT. This results in a signal current of:

$$Signal_{current} = \frac{44\ \mu Vrms}{DUT} = \frac{44\ uVrms}{10\ \mu\Omega} = 4.4\ Arms \quad (8)$$

The 4.4 Arms signal, multiplied by the Thevenin 25 Ω, results in 110 Vrms, confirming the initial solution.

One could consider developing a 40 dB amplifier, but considering the voltage-related dangers to both the user and to the instruments, this is not a viable solution. While the Bode 100 is fast, measuring with a low receiver bandwidth to minimize the noise is not nearly fast enough to perform this testing without including the refrigeration cooling.

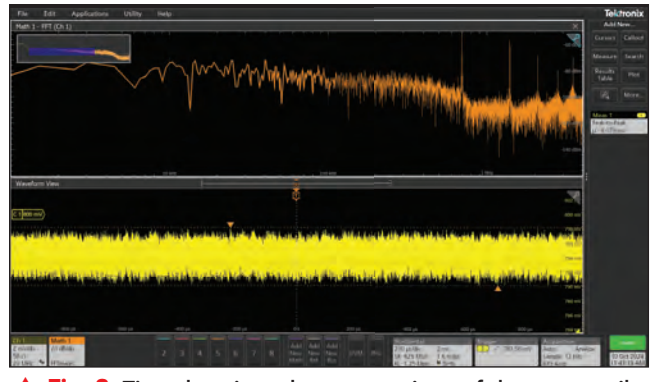

Fig. 3 Time domain and spectrum views of the power rail noise for the 1500 A ICONIC demo board.

Establishing Boundaries

A few ground rules are required before actually defining the measurement solutions. For the purpose of this investigation, use the following conditions:

1. Let the maximum measurement acquisition time of 10 milliseconds (ms) be set arbitrarily. This is generally well within the limits of the Vrms on the power board and the load.
2. The measurement cannot require equipment other than typical validation equipment already commonly available.
3. The frequency range of the impedance measurement is from 1 to 2 kHz to a few MHz.
4. Additional post-processing time is allowed; the 10 ms restriction pertains to running a powered board up to and including its maximum load.

Since most high-power labs use some form of an in-socket load to validate the Vrm performance, this is the tool of choice. Here, a Picotest S2000 high-speed, in-socket, load board solution is used, but devices from other manufacturers should work similarly. The load board is a software-controlled load capable of emulating almost any current profile including pulses, sine waves, and pseudo-random patterns.

With the ground rules established, and after careful consideration, three load current modulation patterns were identified as candidates for this impedance measurement. The Picotest 1500 A ICONIC demo board was selected to power the S2000 load board, since it is very low impedance at about 30 μΩ and is easy to program the different waveforms. Any suitable board and load should be able to perform similarly.

An added benefit of using the load is that minimal current flows in the instrument cables. While this is a small ground loop, most of the current is limited to the loop through the load and power board. Despite this, a TPR4000 power rail probe with a J2115A coaxial isolator and a P2104A browser tip to connect to the board were used (see ***Figure 4***).

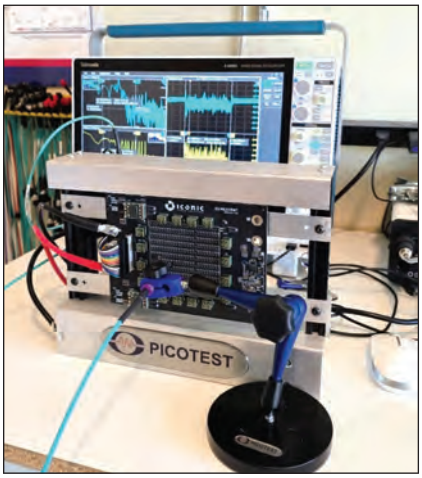

Fig. 4 A picture of the ICONIC demo board with the P2104A 1-port browser probe as well as the Tektronix MSO6B scope with a TPR4000 power rail probe in the background. A second cable is monitoring the programmed load pattern.

The three candidate methods for making this measurement are shown next, with a basic description and commentary in ***Table 1***.

Impulse

The impulse is well-known to have a flat response, or constant amplitude versus frequency, and wide bandwidth. The amplitude at each frequency is set by the pulse amplitude and the pulse duty cycle. The bandwidth is set by the on-time and the impulse repetition frequency, while the minimum frequency and the frequency spacing are set by the impulse repetition rate. This necessitates some compromises to achieve all the goals.

For this example, two sequential double pulses were used. The first two pulses are 1200 A, 5 microseconds (μs) wide and a 500 μs period. The duty cycle is 1%, resulting in an average power less than 10 W. The 5 μs pulse width results in a 3 dB bandwidth less than 100 kHz, which is short of the 1 MHz minimum goal. A second double-pulse is set for a 50 μs period and a 500 ns pulse increasing the bandwidth by an order of magnitude. This also averages less than 10 W. The entire acquisition requires a bit more than 1 ms memory allowing a 2 ms acquisition to capture 1 kHz. A third double-pulse could increase the maximum frequency. The S2000 software interface, showing the double-pulse program, is shown in ***Figure 5***.

Two separate FFTs are performed after the voltage data is captured: one for the lower frequency pulse pair and one for the higher frequency pulse pair. The raw FFT results are shown in ***Figure 6***. The impedance at each frequency is interpreted from the division of the voltage/current.

The impulse is the simplest measurement, requiring only a single level pulse. Achieving a reasonable amplitude requires large duty cycles, reducing the bandwidth. This is overcome by cascading several double pulses and extracting the FFT from each

TABLE 1

SUMMARY OF THE THREE CANDIDATES FOR LOAD CURRENT MODULATION SOLUTIONS FOR THIS 3-PORT V/I MEASUREMENT

Method	*Description*	*Comments*
Multi-impulse	4-6 low duty cycle single amplitude pulses.	This method, being only one level, is also suited to stepper probes.
Stepped sine	Multiple sequential sine waves at different frequencies.	Requires high sample rate and many levels. The slowest and requires the most post-processing, but also presents the largest signals.
Compact-discrete	Many sine signals added together for simultaneous measurement.	Requires high sample rate and many levels.

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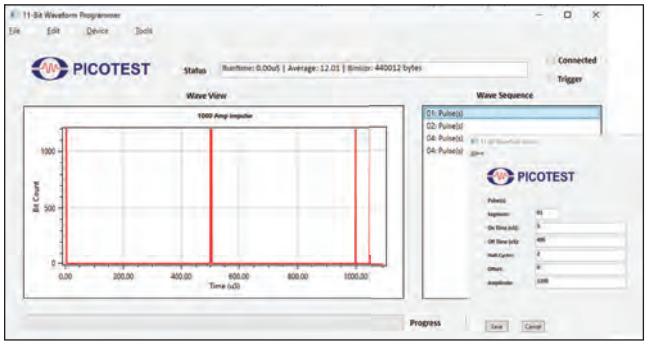

Fig. 5 The S2000 software GUI panel shows the program waveform and the details of one of the pulses.

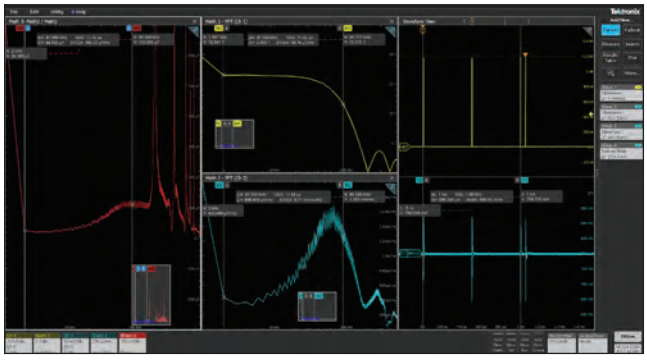

Fig. 6 Raw FFT results of the lower frequency pulse pair and the calculated impedance from the extraction shows 26.2 μΩ.

double-pulse waveform, extending the bandwidth. The post-processing of the FFT data is relatively straightforward from the oscilloscope data, either internally or externally, and it is the lowest average power of all the solutions.

Swept or Stepped Sine

At the opposite extreme, the swept sine methodology is the slowest of the methods and requires the most post-processing, but also offers the largest signals, allowing measurement of the lowest impedance. Due to the very high sample rate of the controller, insufficient memory was available for the 11-bit sine signal at 1 kHz. This method in any case is included, since the controller sample rate will be made selectable to eliminate this limitation. This example includes nine sequential sine waves starting at 5 kHz and requiring 1.4 ms of run time (see ***Figure 7***). At 1 kHz minimum, this would increase to 7 ms. Since higher frequencies will be required, the time will increase, but not significantly, and it will still easily meet the 10 ms criteria.

This example uses nine independent FFTs to demonstrate the first decade of frequencies, though the frequencies are known. Increasing the maximum frequency will increase this to approximately 30 FFTs within the scope. For the purposes of brevity, only one of the raw FFT results (7.5 kHz) is shown in ***Figure 8***. The impedance at each frequency is interpreted from the division of the voltage/current.

The stepped sine is the most complex measurement because of the many individual FFTs required;

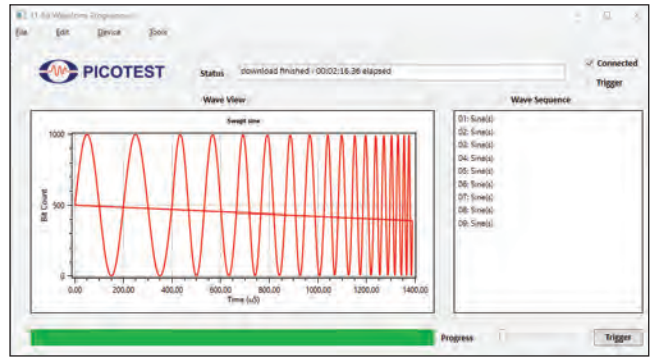

Fig. 7 The S2000 controller software panel showing the nine sequential sine waves. Each consists of two cycles, and each is a 500 A peak with a 500 A offset for a 0 to 1000 A sine wave.

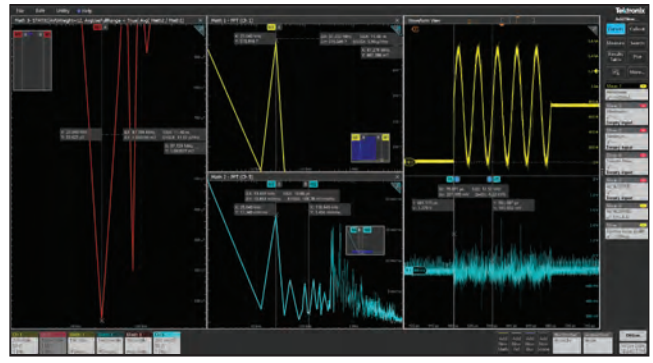

Fig. 8 This method results in the largest signal, 344 A rms at 7.5 kHz is shown here. Two cycles are used at each frequency to obtain an FFT result.

however, this should be simple to automate with each frequency known. As it is all post-processed, the power board is not running aside from the 10 ms of allotted acquisition time. This measurement allows the largest of the signals, but has an average power of 250 W for the measurement duration.

Compact-Discrete Multi-Sine

The third and final candidate is the compact-discrete signal, which is in the class of multi-sine signals. As its name suggests, the single waveform is a complex sum of coherent, non-coincident, discrete sine waves. It has the benefit that it can excite many discrete frequencies with flat response. The signals are larger than the impulse, but this solution requires a high sample rate, high-resolution controller, and load. The process for determining the waveform is highly complex, but it is a built-in selection in the S2000 software controller, or it can be imported from an external CSV file. The GUI panel showing the CSV imported compact-discrete signal is shown in ***Figure 9***.

Like the stepped sine, this solution requires many FFTs; however, this method offers simultaneous FFT acquisition, and the FFT frequencies are known such as in the stepped sine solution, making the post-processing simpler. The maximum signal amplitudes are larger than the impulse and smaller than the stepped sine (see ***Figure 10***).

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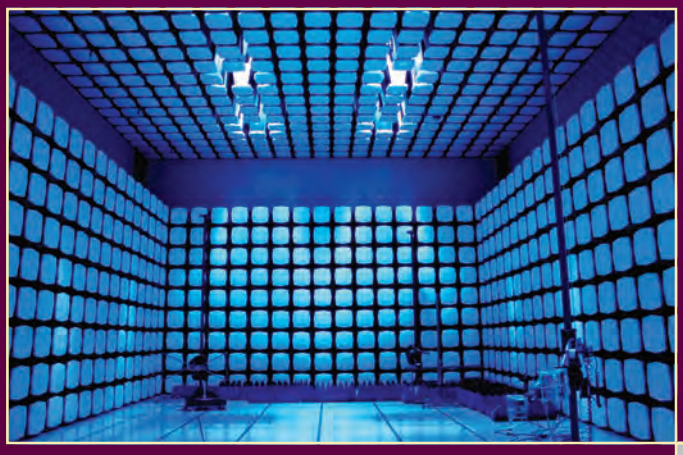

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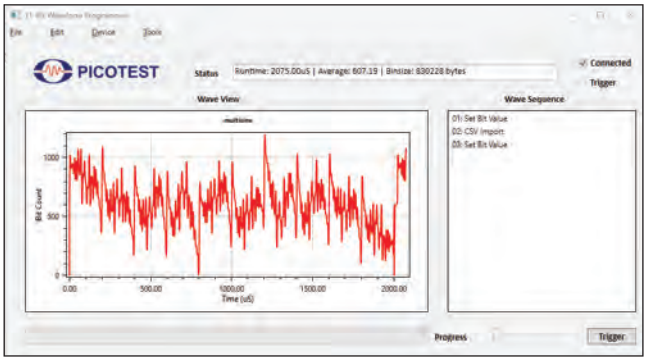

Fig. 9 This compact-discrete signal was imported from a CSV file, but is also available from the pull-down menu for wave segments.

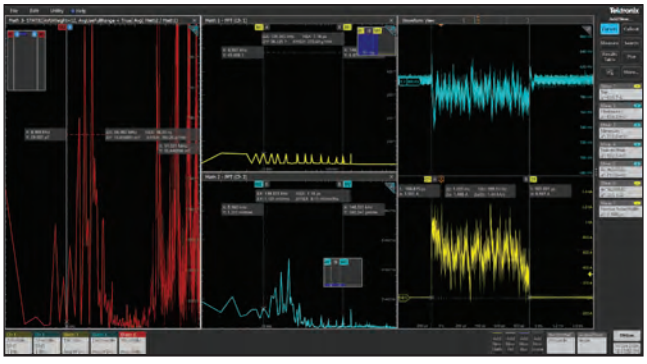

Fig. 10 Raw FFT data from the compact multi-signal pattern on the lower right, and the voltage response on the upper right. The equal amplitude current signals are shown in the lower left with a 45 dBm amplitude. The extract impedance is 29 μΩ.

DC Load Line for Comparison

For reference, the resistance was also measured from the load line as the difference in voltage divided by the difference in current. This results in 42.4 milli-V/1500 A or 28 μΩ (see ***Figure 11***). The division from the rms voltage and current between the cursors is a slightly higher 15.62 milli-V/507.6 A or 30 μΩ. This is a simple and direct measurement, but is only a DC measurement.

The compact-discrete FFT shows the individual frequencies and the flat response, with each signal being approximately 45 dBm. The individual voltage response to each frequency is also shown here. Again, the high sample rate, high-resolution waveform does not allow reaching as low as 1 kHz, but, as with the stepped sine solution, allowing control of the sample rate in the signal generation panel will eliminate this issue. Since the stepped sine solution requires two cycles of the lowest frequency signal, the measurement requires 2 ms acquisition time for a 1 kHz minimum frequency signal. The maximum frequency is set by the load edge speed and the sample rate of the controller. The load speed bandwidth on this board is approximately 40 MHz and the controller sample rate is 66 MSPS. Halving the controller sample rate would allow nearly full bandwidth with a 1 kHz signal, using the maximum available controller memory.

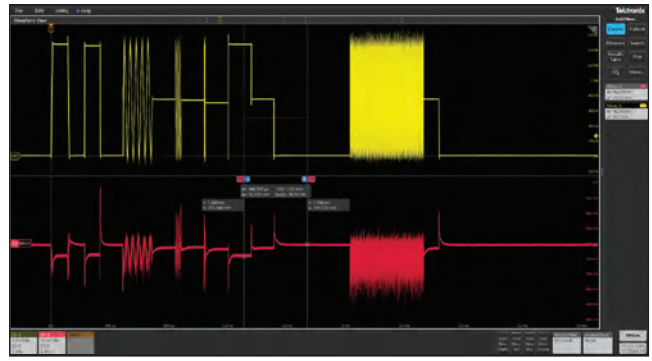

Fig. 11 The load line was measured as the difference in voltage between 0 A and 1500 A, resulting in a load line resistance of 28 μΩ.

Conclusions

In this article, three candidate solutions for measuring ultra-low impedance with a maximum of 10 ms were presented. The methods are compared in ***Table 2***. Though all three methods have pros and cons, they are useful approaches to keep in mind, as each one may serve a purpose at some point in time. All the methods use the same test equipment and setup.

The methods are also compared in Pathwave ADS simulations, which eliminates the effects of noise, measurement errors, and other non-idealities. For this purpose, each signal was applied to a 33 μΩ resistor. The results are shown in ***Figure 12*** and all three were exactly 33.0 μΩ.

Each of these three methods meets the 10 ms measurement goal, even considering the sample rate change needed to allow longer acquisition windows. Any leftover time can be used to measure the power board efficiency, also without the cooling attached. With 100 μs dwell, the efficiency was measured at 13 discrete levels (see ***Figure 13***).

In each case, the controller-programmed current (not the measured current) is multiplied by the output voltage, resulting in Equation 1. This product is divided by the product of the 48 V input voltage and the 48 V input current, which is Equation 2. The efficiency result, Equation 3, is shown in ***Figure 14***. The required dwell time is set by the

TABLE 2

THE RANKING OF THE THREE CANDIDATE OPTIONS FOR THE KEY METRICS

Method	Signal Complexity	Amplitude	Acquisition Time	Post-Processing	Measured
Multi-Impulse	Low	Low	Low	Low	26.2 μΩ
Stepped Sine	Moderate	High	High	High	33.6 μΩ
Compact-Discrete	High	Moderate	Moderate	Moderate	29 μΩ
Load Line	Low	High	Low	None	28 μΩ

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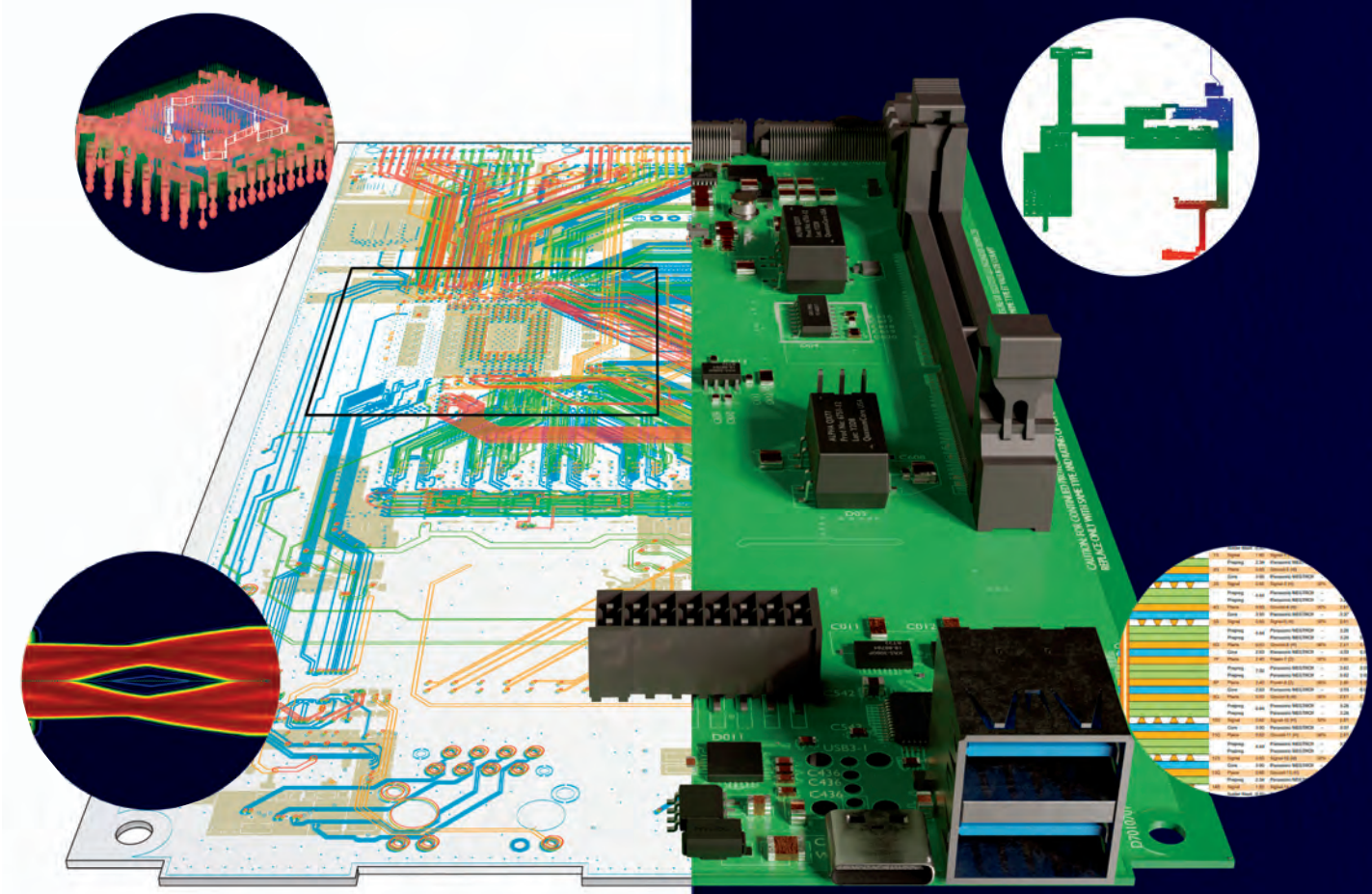

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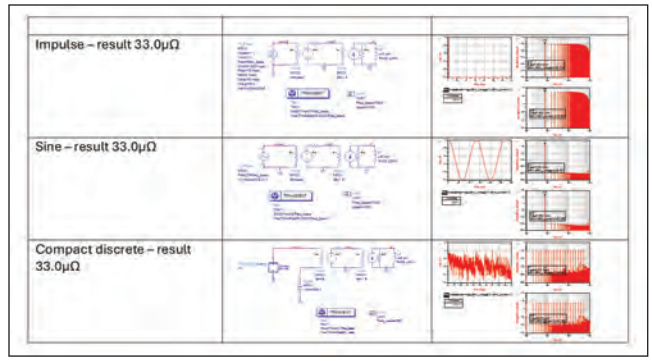

Fig. 12 All three methods are simulated using Keysight Technologies Pathwave ADS and provide the exact result of 33.0 μΩ.

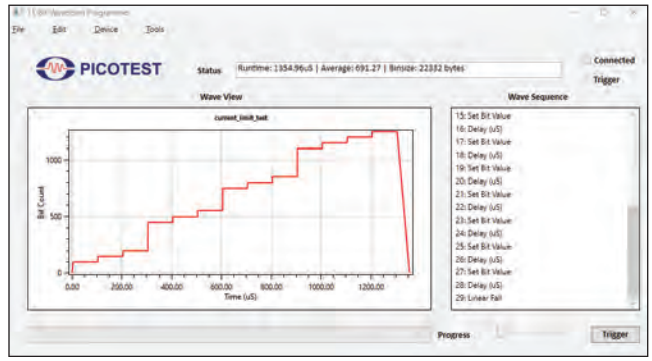

Fig. 13 Discrete current levels are set for measuring efficiency with a 100 μs dwell. The measurement acquisition time is less than 1.5 ms.

Fig. 14 The output current is stepped, and the input power and output power are monitored and divided to provide the efficiency data in a 1.5 ms acquisition without any cooling.

settling time of the input current. The overshoots in the efficiency curve are the results of the evaluation before the settling time and should not be used.

The total measurement acquisition time for the efficiency measurement is approximately 1.5 ms. Improvement in the quality of the measurement could be obtained by averaging a few measurement samples. Six samples could be performed in a 10 ms acquisition time, allowing the efficiency to be measured without attaching the cooling system.

A special thanks to David Sandler. Without his help in developing this controller software and these waveform algorithms, none of this would be possible.

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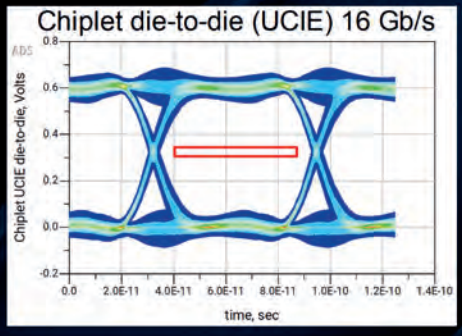

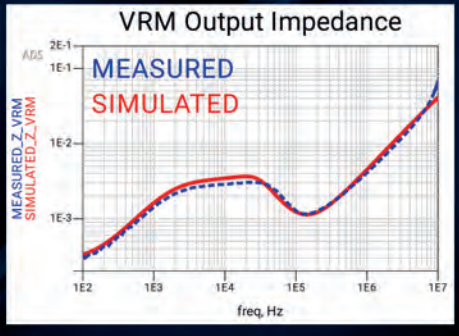

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How Interconnects Work: Crosstalk Quantification

Yuriy Shlepnev, Simberian Inc.

Crosstalk is unwanted noise from structures coupled to a signal link that degrade the useful signal and may reduce the data transmission rate and even cause complete link failure. All possible signal degradation effects, including the crosstalk, can be expressed with the balance of power as follows:

P_out = P_in - P_absorbed - P_reflected - P_leaked + P_coupled

The formula is valid in the time domain and in the frequency domain over the bandwidth of the signal.[1] Here, P_out is the power of signal at a receiver. The power from a driver (P_in) is absorbed in dielectrics and conductors (P_absorbed),[2] reflected back to the driver (P_reflected)[3,4] and, possibly, leaked (P_leaked) to coupled structures. P_leaked is a type of loss that includes local leaks to other signal links[5] and leaks to power distribution systems and radiation that happen mostly at the unlocalized via-holes.[6] The leaked power can be predicted or prevented relatively well; it requires analysis of a link with potentially coupled links (local coupling) and analysis of via-holes with absorbing boundary conditions. Only small leaks on via-holes can be accurately predicted with the analysis in isolation from the rest of the board, and the large leaks must be prevented. Overall, the effects of leakage on a signal can be predicted relatively well in links with vias localized up to a target frequency. This is unlike the last term in the balance of power: the power gained from the coupled structures or P_coupled.

There are a lot of uncertainties related to P_coupled and, as the result, there are multiple ways to characterize it. This is because of a signal from the coupled links or aggressors involved in the analysis.[10] It can be one or multiple aggressors, signals similar to the victim signal as in parallel buses, or signals with different data rates and/or rise time in cases of accidental or distant coupling. Peaks of crosstalk are defined by the aggressor signal; the timing of the peaks and victim signals are not synchronized, but they are not completely random as well. The impact of the coupling also depends on the strength of the signal in the victim link and the location of the coupling. Very small coupling at the victim receiver where the useful signal is already degraded by the absorption and reflection losses may have much greater impact on the signal compared to larger coupling at the driver end of the victim link. As a consequence of that uncertainty, there are multiple ways to quantify the crosstalk phenomenon, and this article discusses most of them. Overall, the crosstalk simulation and quantification can be separated into four categories:

1. Coupling Coefficients: Analysis of transmission line cross-sections at one frequency point and use of approximate equations for backward and

forward coupling (Kb and Kf)

2. Frequency Domain: Extraction of S-parameters with coupling in frequency domain and use of crosstalk metrics PSXT, ICR, and ICN

3. Time Domain: Simulation in time domain with step, pulse or PRBS excitation signals (peak voltages or eye distortion)

4. Probabilistic: Statistical evaluation of crosstalk impact on bit error rate (BER) and channel operating margin (COM).

The first approach, coupling coefficients, is useful only for the evaluation of local coupling in parallel or nearly parallel traces and can be effectively used for quick pre-layout investigations or to find the locations of crosstalk in post-layout analysis. The second approach, frequency domain, is the most universal and is the foundation for the time domain and probabilistic approaches. It can be used for both local and distant coupling.[5] The third approach, time-domain analysis, is also universal and, technically, is the most accurate evaluation of the actual crosstalk values. The time-domain response is usually computed from the frequency domain S-parameters, to account for the frequency-dependent dispersion. But the results are useful on its own, especially for understanding the phenomenon. The time-domain analysis is useful for evaluation of the crosstalk from a step or pulse (single bit or symbol) excitation. It can be used to simulate a crosstalk from pseudo-random bit streams (PRBS), but the bits in a victim signal and the bits in possible aggressor signals are not correlated, and the timing of the rise and fall edges in aggressors and victims are not synchronized; different bit sequences and timing produces different crosstalk impact. To handle these uncertainties, the crosstalk can be treated as a noise with a bounded probability density function identified from the time-domain analysis. The fourth approach is the most modern probabilistic option in terms of aligning with the crosstalk treatment in the IEEE 802.3 and OIF-CEI signaling standards. It may be also the most pessimistic crosstalk model.

Simbeor software is used to generate all examples for this article. Crosstalk validation platform XTALK-28/32 from Wild River Technology is used to illustrate the crosstalk quantification for the post-layout examples.[11]

Crosstalk Quantification with Coupling Coefficients

The fastest and the simplest way to quantify crosstalk is to simulate a cross-section of coupled traces with a field solver at one frequency point and use approximate equations for evaluation of forward and backward coupling. With this approach, capacitance (C) and inductance matrices per unit length are computed for a cross-section with the coupled traces first. Then an equation is used to evaluate possible backward (Kb) and forward (Kf) coupling coefficients for a transmission line segment with length, l, for a step signal with unit amplitude and rise time, t_r. Jarvis derived such formulas[7] for single-ended symmetric traces. The Jarvis formulas were further improved for small segments and for non-symmetric coupling cases by Bracken[8]:

$$K_B = \frac{l}{2(T_1 + T_2)} \cdot \left(\frac{L_{21}}{\zeta_1} - \zeta_2 C_{21} \right) \cdot \min\left(1, \frac{T_1 + T_2}{t_r}\right) \quad (1)$$

$$K_F = -\frac{l}{2 \cdot \max(|T_1 - T_2|, t_r)} \left(\frac{L_{21}}{\zeta_1} + \zeta_2 C_{21} \right) \quad (2)$$

Here, C_{21} and L_{21} are mutual capacitance and inductance, T_1 and T_2 are flight times, and ζ_1 and ζ_2 are impedances of the coupled traces or impedances of differential modes for differential traces. The coefficients are the voltage step responses at the near-end (Kb) and the far-end (Kf) of the coupled transmission line segment, assuming 1 V step excitation in the aggressor. If only one coupled segment is involved, Kb is the voltage of near-end crosstalk (NEXT) and Kf is the voltage of far-end crosstalk (FEXT). The equations are relatively accurate for lossless or low loss cases. However, they do not work well with high losses or long segments (it may overestimate the forward crosstalk that is attenuated by the losses).

The formulas can be used as an estimate of the maximal possible step crosstalk. The formulas also assume ideal transmission line segment termination and do not account for possible reflections (yes, the crosstalk is reflected, too). Note that the reflected NEXT can be observed as FEXT and the formulas provided above can be further improved.[9] However, the frequency or time-domain simulation of crosstalk is always preferable to account for the reflections. Additionally, it should be noted that the step excitation may underestimate the actual peak-to-peak crosstalk for short links by up to 2x or by up to +6 dB.

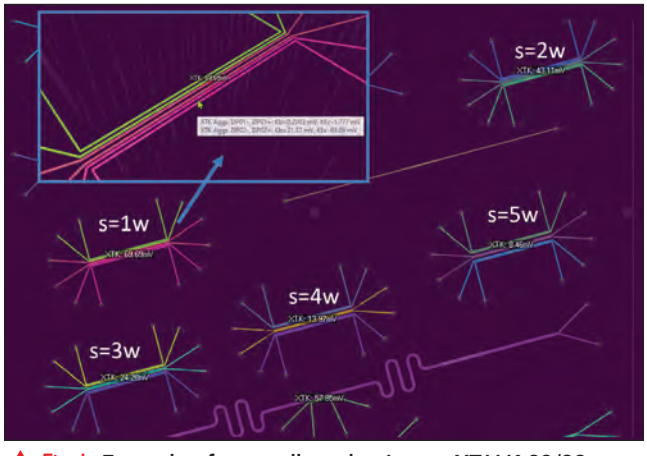
The coupling coefficients is a convenient tool for both pre-layout and post-layout crosstalk investigation. Different kinds of sweeps can be used to define design rules in the pre-layout process for instance. A static or quasi-static field solver is needed to begin such an investigation (such as Simbeor SFS, available in Simbeor software). This can be done by scripting in MATLAB or Python and using the Simbeor SFS field solver through Simbeor SDK.[10]

The coupling coefficients can be used for preliminary investigation of an existing PCB layout to find the location where the coupling coefficients exceed some threshold. It can be done with one button click using the advanced simulation-based Electrical Rule Checking (ERC) mode in Simbeor SI Compliance Analyzer tool (only signal rise time is required for this type of analysis). The crosstalk validation platform XTALK-28/32 from Wild River Technology is a

perfect tool to validate and illustrate different ways to analyze the crosstalk. (This is in addition to the investigation of interconnects predictability with the analysis to measurement correlation). The results of the crosstalk analysis for four 2-in. coupled differential segments and long link coupled to short link are shown in ***Figure 1***. The insert shows details of the crosstalk evaluation for a 2-in. structure with 1w separation between the pairs; the forward coupling Kf = -69.69 mV dominates the backward coupling Kb = 21.37 mV for the bottom differential pair. The stackup for the XTALK-28/32 board[11] is practically the same as for the CMP-28 validation platform featured in[12]. Trace widths are 13.5 mil (wide traces are used to reduce the effect of manufacturing variations). As can be seen in Figure 1, the larger separation results in less coupling.

Crosstalk Quantification in Frequency Domain

A more accurate way to quantify the crosstalk is to simulate a segment of multi-conductor transmission line in frequency domain over a signal spectrum bandwidth. S-parameters of a coupled line segment can be either extracted separately for an analysis in isolation (to generate rules in pre-layout process) or used as an element of a model for coupled links that contains segments of coupled traces. Note that the S-parameters with coupling can be directly used to quantify the crosstalk. For instance, a transmission parameter between two ports from different links is a coupling parameter that describes the crosstalk. S-parameters of coupled links can be directly used to simulate the effect of coupling in time domain or evaluate the probability density function of crosstalk.[13,14] Though, a metric called Power Sum Crosstalk (PSXT) may be useful for preliminary evaluation of overall crosstalk in a link with multiple aggressors.[13] It can be defined as follows (for additional information, please refer to OIF-CEI and IEEE 802.3 standards):



▲ Fig. 1 **Example of crosstalk evaluation on XTALK-28/32 platform in Simbeor SI Compliance Analyzer for five 2-in. differential microstrip structures with the edge-to-edge separation from 1 to 5 trace widths and for long to short link coupling structure (bottom), 25 ps rise time (10% to 90%).**

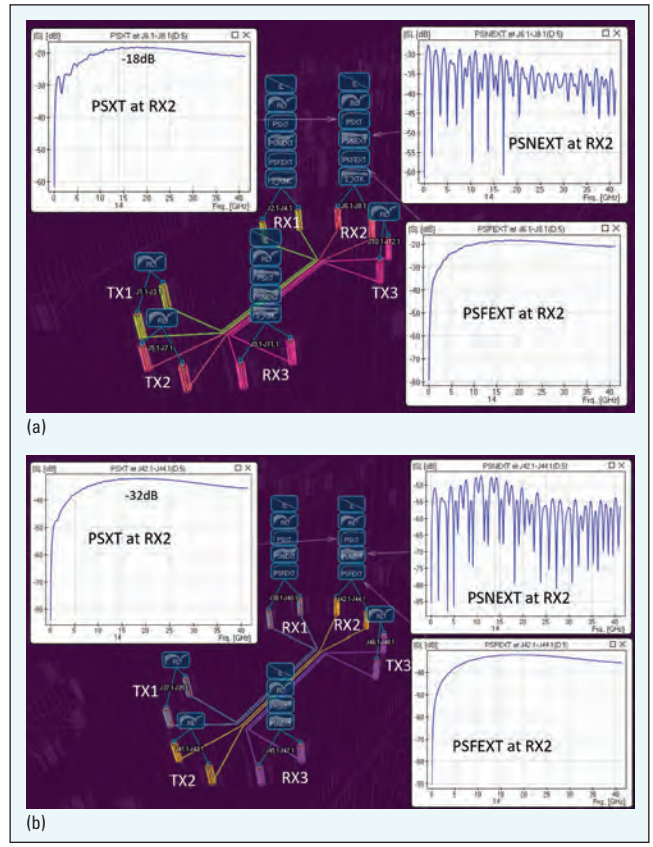
$$PSXT_i = 10 \cdot log\left(\sum_{j\varepsilon\Omega_{XT}} |S_{i,j}|^2\right)[\mathrm{dB}] \quad (3)$$

$$PSNEXT_i = 10 \cdot log\left(\sum_{j\varepsilon\Omega_{NEXT}} |S_{i,j}|^2\right)[\mathrm{dB}] \quad (4)$$

$$PSFEXT_i = 10 \cdot log\left(\sum_{j\varepsilon\Omega_{FEXT}} |S_{i,j}|^2\right)[\mathrm{dB}] \quad (5)$$

PSXT is the total power sum crosstalk. PSNEXT and PSFEXT are PSXTs from the near- and far-end aggressors. PSXTs are functions of frequency and are computed from the S-parameters at a set of frequency points. The PSXT is just a sum of squares of S-matrix elements from all possible aggressors at a victim receiver port, expressed in dB. If there is just one aggressor, PSXT sum contains one S-parameter element. In this case, PSXT is equal to corresponding S-parameter magnitude, expressed in dB. PSXT is different from S-parameters only if there are multiple disturbers or aggressors. In such cases, PSXT may be called Multiple Disturber PSXT (MDXT, MDFEXT, and MDNEXT, respectively).

As an example of the post-layout crosstalk analysis, let's compute PSXTs for some differential coupled links from XTALK-28/32 platform. Very similar to ERC, it can be done with one button click in Simbeor SI Compliance Analyzer tool (either Fast SI or 3D EM analysis can be used for the crosstalk modeling). However, this requires additional setup for the transmitters and receivers in order to properly



▲ Fig. 2 **Examples of post-layout PSXT analysis on XTALK-28/32 platform in Simbeor SI Compliance Analyzer for 2-in. differential microstrip structures with the edge-to-edge separation equal to a) 1 trace width and b) 4 trace widths. TX1-TX3 are the transmitter sides and RX1-RX3 are the receiver sides.**

define victims and aggressors. The bit rate and rise time must be also defined; the frequency sweep is auto-defined from these data, but it can be manually re-defined, if necessary. Simbeor uses decompositional electromagnetic analysis[15] that accounts for the coupling between transmission lines.

The results of PSXT analyses for two structures with three differential links coupled over 2 in. parallel segments are shown in ***Figure 2***. Those are two structures from Figure 1 marked as s =1w and s = 4w. The differential trace width is 13.5 mil and the differential trace pitch is 37 mil. Those are loosely coupled microstrip differential pairs, which are very susceptible to interference, as we can see from these examples. In each case, two links have transmitters on one side (TX1 and TX2) and one link has transmitter on the opposite side (TX3). Each receiver has multiple disturbers, in this case. Crosstalk on the victim receiver (RX2) is also shown in Figure 2. RX2 has one near-end aggressor, TX3, and one far-end aggressor, TX1. As in the case of pre-layout example, the corresponding PSNEXT and PSFEXT are exactly the magnitudes of corresponding transmission parameters. The total PSXT is the sum of squares of magnitudes expressed in dB. PSXT is a superposition of the aggressor's signals and does not account for the phases of signal harmonics. The PSFEXT dominates in both cases. PSNEXT is also substantial for the case with smaller separation between coupled differential pairs.

The s =1w case has maximal PSXT of about -18 dB, or about 126 mV. The s = 4w case has maximal PSXT of about -32 dB, or 25 mV. It is an estimate of the superposition of the crosstalk with two aggressors (near- and far-end). Figure 1 shows only the largest values of the forward or backward coupling. Note that the ERC mode does not account for the actual signal propagation direction and assumes no reflections. The model used for PSXT computation does not have such limitations.

PSXT can be used to evaluate the crosstalk and set the limits or verify compliance for some signaling standards that provide compliance masks specifically for PSXT. The same level of PSXT may

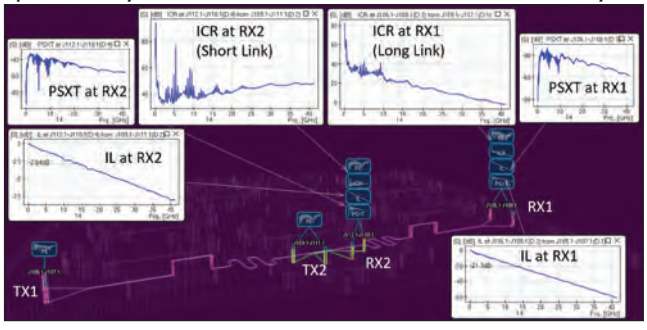


Fig. 3 **Examples of post-layout ICR analysis on XTALK-28/32 platform in Simbeor SI Compliance Analyzer for long and short coupled links. TX1-RX1 is the long link and TX2-RX2 is the short link. ICRs for both receivers are shown at both receiver ports together with corresponding PSXT and IL.**

be acceptable for a link with small losses, but cause failure in a link with large losses. Insertion loss to crosstalk ratio or ICR metric can be used to evaluate and quantify the impact of the crosstalk on a particular link:

$$ICR_{i,j} = IL_{i,j} - PSXT_i\,[\mathrm{dB}] \tag{6}$$

where $IL_{i,j} = 20 \cdot log\,(|S_{i,j}(f)|)$ is the insertion loss at port i and $PSXT_i$ is the power sum crosstalk at the same port (both values are expressed in dB).

ICR is a king of signal to noise ratio[13] (IL is the signal at a receiver and PSXT is the noise). The larger values of ICR mean smaller impact of the crosstalk on the signal. To understand the ICR, let's use structure with coupled long and short links from XTALK-28/32 platform. The results of the analysis are shown in ***Figure 3***. ICR at RX1 is computed for longer link, and ICR at RX2 is computed for the shorter link. It can be observed that the shorter link has much larger ICR, which means smaller impact of the crosstalk. This is because of much smaller insertion loss in the shorter link. PSXT and IL for both links are also shown in Figure 3 for comparison.

The PSXT and ICR are useful metrics for a preliminary crosstalk evaluation. However, those are pure frequency domain metrics. The actual amount of crosstalk noise for a particular signal depends on the signal spectrum and may be also altered by filtering properties of a transmitter and a receiver package. Integrated crosstalk noise (ICN) metric was introduced to account for the signal spectrum and filtering properties of a transmitter and a receiver.[13] ICN is just RMS of weighted PSFEXT and PSNEXT, computed as follows:

$$\sigma_{XTK} = \sqrt{\sigma_{NEXT}^2 + \sigma_{FEXT}^2} \tag{7}$$

$$\sigma_{NEXT} = \sqrt{2 \cdot \Delta f \cdot \sum_k W_{NEXT}(f_k) \cdot 10^{\frac{PSNEXT(f_k)}{10}}} \tag{8}$$

$$\sigma_{FEXT} = \sqrt{2 \cdot \Delta f \cdot \sum_k W_{FEXT}(f_k) \cdot 10^{\frac{PSFEXT(f_k)}{10}}} \tag{9}$$

The frequency-dependent weights W_{NEXT} and W_{FEXT} account for spectrum of random bit sequence. They are computed with the rise and fall time of the near- and far-end transmitters (aggressors), baud rate (bit or symbol rate), reference receiver and transmitter bandwidth, and amplitudes of the near- and far-end aggressors.[13] The result of the ICN computation is near-end σ_{NEXT}, far-end σ_{FEXT}, and total crosstalk σ_{XTK} estimated in volts (rms value). The total ICN is one number that is very convenient for qualitative assessments of the crosstalk impact.

The limit on the ICN is usually set and plotted versus the insertion loss at the Nyquist frequency. An example of ICN computation and plotting for three differential links coupled over 2-in. length with 4 widths separation between the differential pairs is shown in ***Figure 4***. The ICN values are

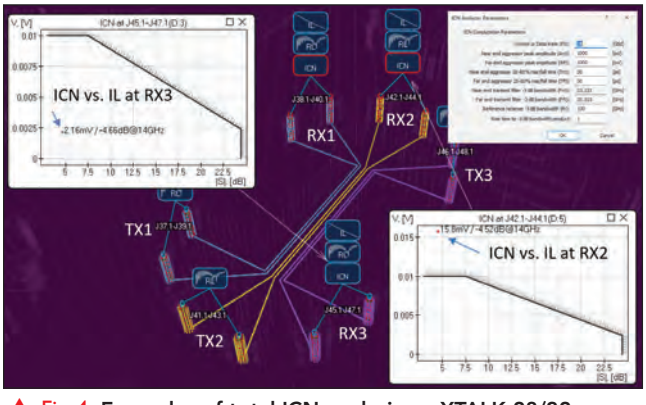
plotted together with a typical compliance mask. The mask allows larger crosstalk in links with smaller insertion losses. The aggressor signals are set to 1 V, in this case; the other parameters for computation of ICN are shown in Figure 4. It can be observed that the receivers RX3 and RX2 have almost the same insertion losses at Nyquist frequency, but the crosstalk at RX2 is larger; the corresponding dot is in the failure area of the compliance mask. In this case, RX3 has only near-end crosstalk from two transmitters, TX1 and TX2. Receiver RX2 has both far-end crosstalk from TX1 and near-end crosstalk from TX3. Note that the ICN is sometimes explained as an average value of expected crosstalk, or even as a standard deviation for a crosstalk with the normal probability distribution.[13] Thus, it is usually the bottom estimate.

Crosstalk Quantification in Time Domain

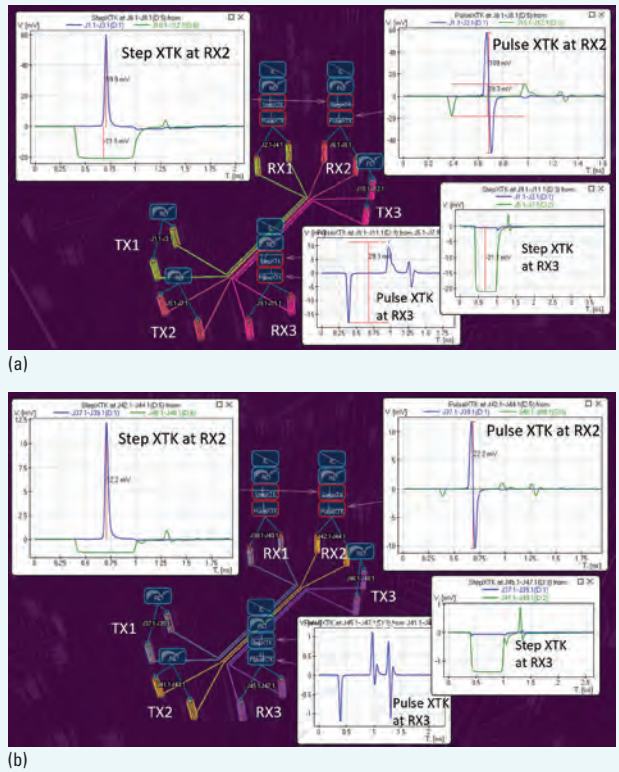
Yet another way to quantify crosstalk is to compute the step or pulse response of a link with coupling and measure the crosstalk values directly in time domain as maximal peak-to-peak value of a voltage response at a victim input/output (IO) with a stimulus attached to the aggressor transmitter IO. This type of analysis can be done with more realistic models of the transmitter and receiver, and also accounts for the reflections from non-ideal terminations. Additionally, the analysis of a victim link in time domain with one or multiple aggressors is useful to understand the "evasive" nature of the crosstalk. If the aggressor signals are not synchronous with the victim signal, the crosstalk does not correlate in time with the single bit response.[5] Thus, it cannot be mitigated as the other types of signal degradation factors such as reflection and losses. The time-domain analysis in Simbeor is done with the rational approximation of S-parameters computed for a segment or a complete link.

As an example of the post-layout crosstalk analysis, let's simulate differential coupled links from the XTALK-28/32 platform that were previously investigated with coupling coefficients and frequency domain. (Again, it can be done with just one button click in the Simbeor SI Compliance Analyzer tool). However, in addition to setting up the transmitters and receivers, time-domain stimuluses should be defined before the crosstalk simulation. The minimal setup requires the bit rate and rise time. Amplitudes of the sources, type of bit stream, and possible jitter parameters may also need adjustments.

The results of step and pulse crosstalk analyses for two structures with three differential links coupled over 2 in. parallel segments are shown in ***Figure 5***. Those are two structures from Figure 1 marked as s = 1w and s = 4w. Differential trace width is 13.5 mil and differential trace pitch is 37 mil. In each case, two links have transmitters on one side (TX1 and TX2) and one link has a transmitter on the opposite side (TX3). The pulse and step crosstalk are shown at receivers RX2 and RX3. RX2 has two aggressors: far-end, TX1, (blue lines on the plots) and near-end, TX3 (green lines on the plots). RX3 has two near-end aggressors, TX2 and TX1. Overall, crosstalk at RX3 is much smaller compared to RX2. Also, the far-end crosstalk at RX2 dominates, which is consistent with the investigation in frequency domain that was shown in Figure



▲ Fig. 4 Examples of total ICN analysis on XTALK-28/32 platform in Simbeor SI Compliance Analyzer for 28 Gbps signal in 2-in. differential microstrip structure with the edge-to-edge separation between differential pairs equal to 4 trace widths. TX1-TX3 are transmitter sides and RX1-RX3 are receiver sides.



▲ Fig. 5 Examples of post-layout time-domain crosstalk analysis with step and pulse responses (25 ps rise time) on XTALK-28/32 platform in Simbeor SI Compliance Analyzer for 2-in. differential microstrip structures with the edge-to-edge separation equal to a) 1 trace width and b) 4 trace widths. TX1-TX3 are the transmitter sides and RX1-RX3 are the receiver sides.

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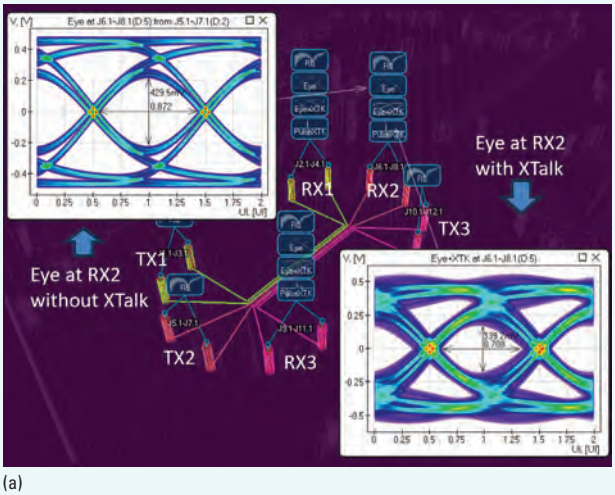
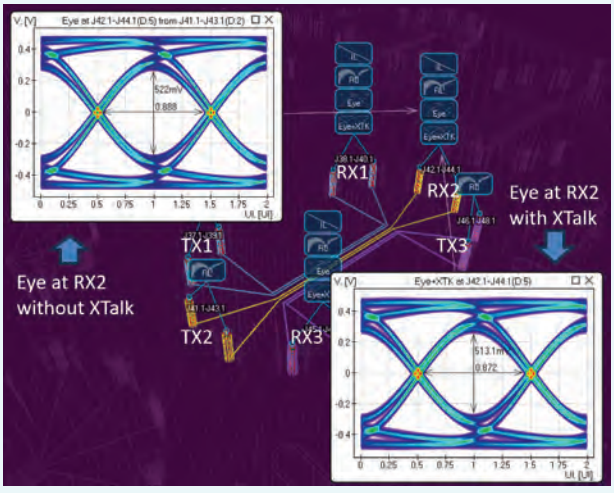
2. Notice that the peak-to-peak far-end crosstalk computed from the pulse response is almost 2x larger than computed from the step response. It peaks at the rising and falling edge of the pulse. However, this is not always the case, and each coupled link should be simulated to find actual values of the crosstalk. Considering the crosstalk values, it can be observed that the FEXT peak-to-peak value is about 110 mV while the NEXT is about 30 mV for the structure with 1width separation between the differential links. Both are below the "upper limit" 126 mV evaluated from PSXT. A possible superposition of the FEXT and NEXT peaks provides a new upper boundary of 140 mV for the crosstalk. The value is specific to the rise time and happens when the peaks of crosstalk from the NEXT and FEXT aggressors coincide in time; it is highly unlikely, but possible.

The step and pulse response may be useful for a preliminary quantification of the crosstalk and the upper bound evaluation. The actual signals in the links are sequences of bits for NRZ/PAM2 signal or symbols for PAM4 signals; eye diagrams are typically used to evaluate the signal distortion. Examples of eye diagrams with and without crosstalk computed at RX2 for two links, with different separations between the links, are shown in ***Figure 6***. The crosstalk impact on the eye is clearly visible in case of strong coupling (see ***Figure 6a***). The eye height is reduced by about 90 mV and the width by about 0.16 of UI. This is below our upper bound estimate 140 mV; this particular sequence of bits did not include the worst-case condition that could produce ideal superposition of the FEXT and NEXT peaks at the middle of the victim eye. A smaller reduction of the eye size is observed for the links separated by 4 widths (see ***Figure 6b***); about 10 mV reduction in eye height and about 0.016 UI reduction in width. In both cases, crosstalk is observed as additional jitter (eye width reduction) and amplitude noise (eye height reduction). That is not the worst case as well.



(a)



(b)

▲ Fig. 6 **Eye diagrams at RX2 without and with crosstalk, computed in SI Compliance Analyzer for 2-in. differential microstrip structures from XTALK-28/32 platform with the edge-to-edge separation equal to a) 1 trace width and b) 4 trace widths. 28 Gbps, 20 ps rise/fall time (10% to 90%).**

In this example, the eyes were computed directly in time domain, with PRBS32 bit stream signals in the victim as well as in the receivers. The sequences of bits in different links are not correlated and the phase or time offset of the bit rise times is defined randomly at the beginning of the analysis. The result of such analysis will depend on the particular phase and bit sequence, as illustrated in ***Figure 7***. The top time domain plot shows a small subset of bits at the receiver ends in three coupled links. The bit sequences are not correlated and the offset between switching time is selected randomly at the beginning of the analysis. At RX2, the useful signal and the crosstalk noise are shown in the bottom plots in Figure 7. The peaks in the noise are defined by the bit sequences and timing in the aggressors, which are not correlated with the victim signal. As a result, peak crosstalk can be observed at any time within the eye, as illustrated by eye diagrams. All graphs show the eye diagrams without the crosstalk. The eye diagram with the crosstalk for that case is shown in Figure 6a. Some bit sequences and timing offsets may degrade the eye more, and some may degrade the eye less. In fact, the crosstalk may even improve the eye opening or reduce the jitter. This is possible, but highly unlikely. In this case, the probability of the worst case is of more interest than the chance of improvement, and statistical methods should be used to quantify this.

Statistical Crosstalk Quantification

The frequency and time domain analyses of the crosstalk are useful tools, but the ultimate metric for a link performance is the BER or eye diagram

height at a specified BER. Statistical methods are usually used to evaluate BER or the eye diagram opening. The statistical approach to the BER evaluation requires a statistical model for a crosstalk. However, the crosstalk is not random in general and is bounded by our worst-case estimates. A possible superposition of the victim signal with crosstalk from two aggressor links is illustrated in ***Figure 8***.

This is the same middle link case with two aggressors as seen in in Figure 6a. The near-end crosstalk looks like a noise, but the far-end crosstalk does not look like a random signal. What is the probability to have the peak noise from FEXT and NEXT? Using time-domain analysis, the probability density function (PDF) can be evaluated for both cases, as shown in ***Figure 9***. PDFs are computed for the tightly coupled links (s = 1w, top plots) and for loosely coupled links (s = 4w, bottom plots). It can be observed that the NEXT distribution looks like normal; this is similar to what is observed in Reference 13. It is getting more "normal" for the loosely coupled links, though the normality test is required to evaluate it. However, the FEXT distribution does not look as normal at all (as seen in the PDFs on the left side in Figure 9) and the probability to have maximal possible values is not negligible. Both distributions are bounded by the maximal possible values for a particular rise time. Though the NEXT and FEXT are independent, as the total crosstalk PDF is a convolution of the two distributions, it is also bounded by the maximal possible value observed from the pulse crosstalk analysis.

The PDFs of the crosstalk can be used to evaluate the effect of the crosstalk on BER or on detector error rate (DER), which is the COM.[13,14] This is the most "modern" method of the crosstalk quantification and may be considered as the next step in evolution of the crosstalk quantification. COM[13,14] is a signal to noise ratio defined as follows:

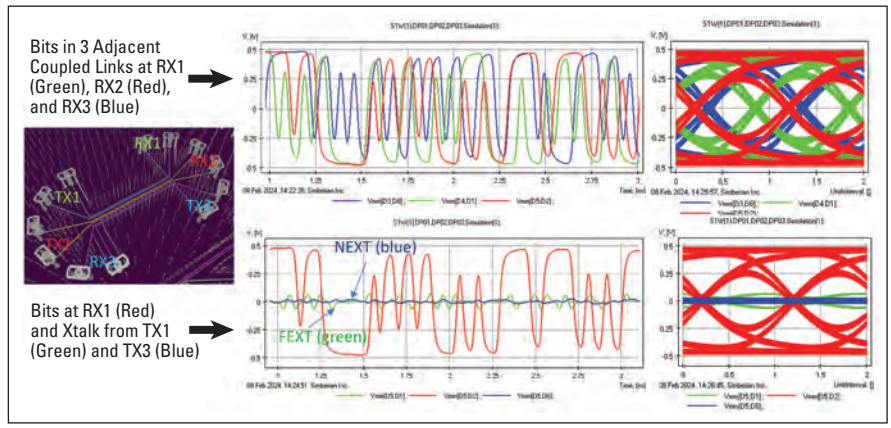


Fig. 7 **Signal and crosstalk superposition example. Bit sequences in three links are shown in top plot and the corresponding eye diagrams are shown on the right for 28 Gbps PRBS32, 20 ps rise/fall time (10% to 90%). The bottom plot shows bits at RX2 and the crosstalk noise from bits in the coupled links alongside the corresponding eye diagram, which depicts the location of the crosstalk noise.**

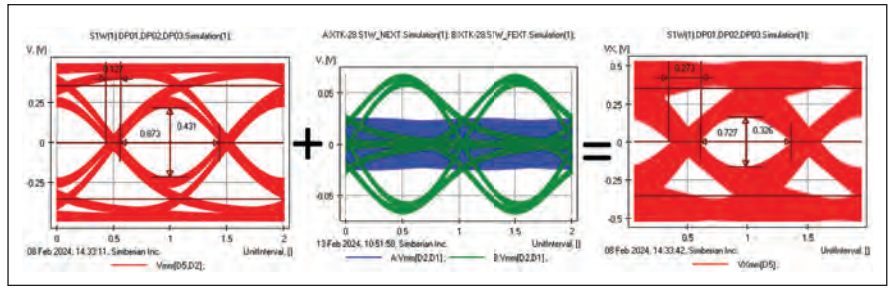


Fig. 8 **Signal and crosstalk superposition example. The following are depicted: an eye diagram without crosstalk (left), near and far end crosstalk components from the aggressor links (middle, where green is FEXT and blue is NEXT), and a plot displaying possible superposition of signal and crosstalk noise (right).**

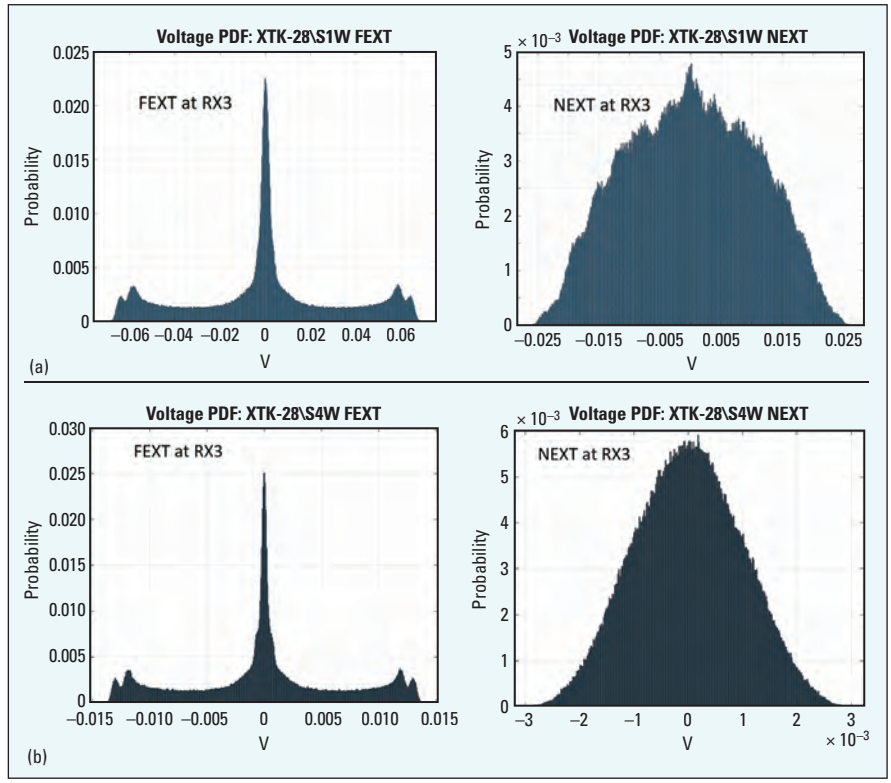


Fig. 9 **Crosstalk probability density functions for 2-in. differential microstrip structures from XTALK-28/32 platform with the edge-to-edge separation equal to a) 1 trace width and b) 4 trace widths. 28 Gbps, 20 ps rise/fall time (10% to 90%), PRBS32, time step 2 ps.**

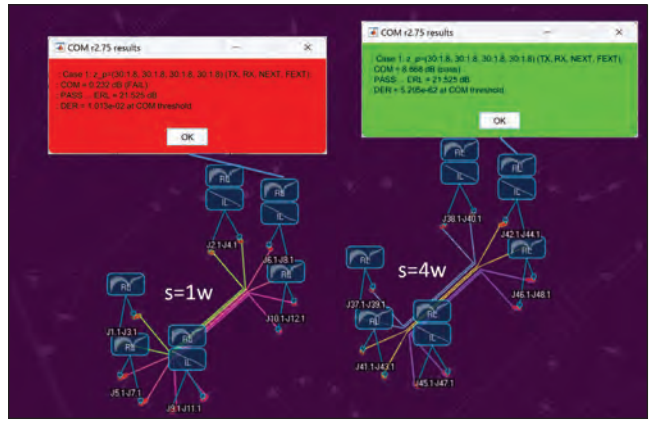
$$COM = 20 \cdot log\left(\frac{A_{Signal}}{A_{Noise}}\right) \quad (10)$$

Where A_{Signal} is the peak signal and A_{Noise} is the peak BER or DER noise defined through the peak signal minus the peak eye opening at a specified BER/DER level. "Signal" in this context includes all losses and dispersion in the link from chip to chip and the effect of equalization. It includes the reference transmitter and receiver models as well. "Noise" in this context includes all possible signal degradation effects with some assumptions. It includes absorption losses and dispersion, return loss, reflections and crosstalk as well as equalization by TX and RX. The COM metric is computed in the time domain as the voltage ratio of signal available in a reference signaling architecture (TX and RX) to noise at the reference receiver's sampler; essentially, it characterizes the complete link from chip to chip. The noise is calculated for the specified DER. DER is a generalization of BER for NRZ and of SER for PAM4. Equalized single bit or symbol responses of the signal link and crosstalk aggressor links are used to calculate the vertical slice of the eye diagram centered at the sampling point where the DER is minimal. The crosstalk in COM is assumed to be in the middle of the eye, but that is highly unlikely.

To evaluate the crosstalk contribution, COM uses S-parameters of the crosstalk paths. The crosstalk in COM is treated as an additional bounded uncorrelated noise similar to the inter-symbol interference. For each crosstalk source, COM computes PDFs and convolves them with the bit PDF to compute the overall crosstalk effect. An example of such analysis is shown in ***Figure 10***. The IEEE COM tool was used for this computation with default reference transmitter and receiver parameters. In this case, the limit of the DER is 1e-4 and the pass value of the COM is 3 dB. As seen in Figure 10, the middle link with 4 widths separation between differential links has a COM of about 8.7 dB. However, the eye at DER = 1e-4 would be almost completely closed if the links have only 1 width separation. The eye closure due to the crosstalk is highly unlikely in this case. Thus, the COM is, probably, the most pessimistic crosstalk metric.

Conclusion

As Ransom Stephens perfectly stated, "The crosstalk problems are back."[16] They are here to stay as long as interconnects are designed as the open waveguiding systems. Thus, understanding and proper quantification of the crosstalk and mitigation of the consequences are important. This article outlines mulitiple possible ways to quantify the crosstalk: coupling coefficients, frequency domain metrics, time-domain analysis of crosstalk, and a modern statistical approach. The ultimate metric of the crosstalk effect



▲ Fig. 10 **Example of COM computation for 2-in. differential microstrip structures from XTALK-28/32 platform with the edge-to-edge separation equal to 1 trace width (left) and 4 trace widths (right). 28 Gbps signal; all other parameters are from IEEE 802.3 spreadsheet.**

is the reduction of BER due to crosstalk. The local crosstalk is deterministic, but usually treated as a part of bounded uncorrelated jitter. This is because of the uncertainties in timing between the victim and aggressor signals. The most modern methods are statistical and are applicable to both local and distant crosstalk evaluation.

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Analysis of Skew

Gustavo Blando and Prashant Pappu, Amazon Web Services

What is Skew?

If someone responded quickly, they might say that skew is the difference in delay (arrival time at a destination) between two signals. However, let's consider this more closely. Imagine there are two traces with the same propagation delay and length, but one of the traces encounters a discontinuity that slightly alters its rise time. In this scenario, the two signals might transition at slightly different times, not just because of the discontinuity itself, but also because the timing difference now depends on the selected threshold, as illustrated in ***Figure 1***. In this context, this requires a deeper consideration of skew: what it is, how it is measured, its significance depending on the context, and ultimately, which definition to adopt.

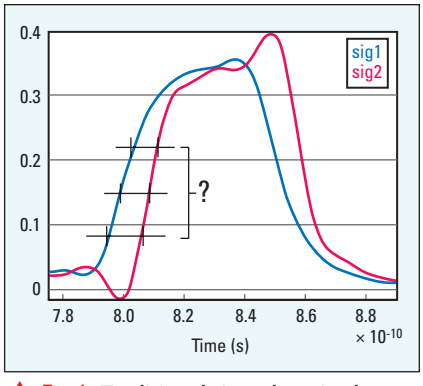

Fig. 1 **Traditional time domain skew definition.**

Taking a step back, it is important to note that skew plays a crucial role in the loss/timing budget for the following reasons:

- In serial channels, skew can degrade the signal and manifest in the frequency domain as increased insertion loss and even dips in insertion loss for large skew values.
- In synchronous channels, it can distort the differential crossing and affect setup-hold times.

As frequencies increase, these distortions may become more pronounced. For instance, a 112G PAM-4 signal has a fundamental frequency of 28 GHz and a bit time of around 18 ps. A seemingly minor 1.8 ps of skew would represent 10% of the unit interval, considering 224G PAM-4 raises concerns that could lead to significant issues.

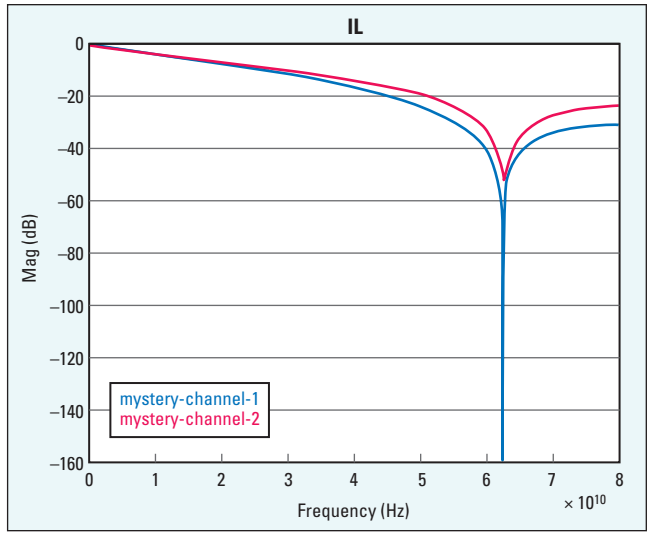

Fig. 2 **Equivalent mystery channels.**

Before delving into the specifics of different skew measurements, it is helpful to illustrate the importance of skew by creating a channel.

Equivalent Channel

Let's try this exercise. In ***Figure 2***, if the question is posed of whether the channels are similar, what would the response be? These two channels look very similar. However, as illustrated in ***Figure 3***, one channel is a differential pair (without coupling) featuring a small stub and no skew, while the other is a differential pair with skew.

Skew can manifest in ways that are easily confused with various other distortions in a skew-less channel. Here is a perspective on it:

- In a single-ended signal, various "bad" elements create distortions such as losses, reflections and dispersion.
- When multiple lines are introduced, as in a differential pair, all the additional distortions that can occur between the signals are added to that list. Skew is simply one of those factors.
- This added "bad stuff" can behave similarly to many other common distortions, as illustrated in the equivalent channel.

The concept of skew is broad, but when discussing very small skew values, it typically refers to the skew between the two legs of a differential pair, known as intra-pair skew. Let's examine how skew has traditionally been measured, along with its advantages and challenges.

Frequency Domain Definition

When skew is being discussed in general, it is important to note that for coupled transmission lines, such as those in differential pairs, in-pair skew is calculated not only by the "difference in delay" of each individual line, but also by considering the cross-coupling from the adjacent signal. Essentially, the skew definition for single-ended traces without coupling is based solely on the difference in phase delay for each leg in isolation. However, in a differential pair, there is likely some degree of coupling, which complicates the skew definition.

In coupled structures, skew is defined as the difference in odd mode delay for each line, as illustrated by the equation in ***Figure 4***. The key takeaway is that once the signal is processed appropriately, the methods for measuring skew are generic; they simply need to be applied to the correct post-processed waveform.

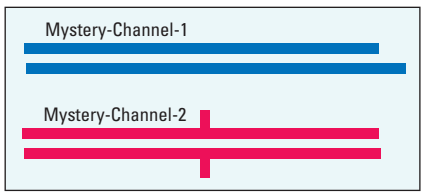

Fig. 3 **Mystery channels revealed.**

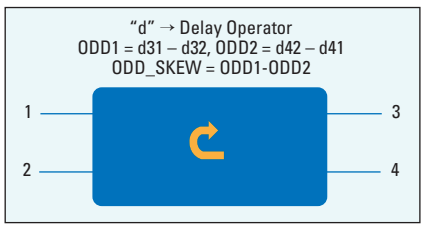

Fig. 4 **Odd skew calculation.**

Since it has been established that the methods for measuring skew are generally applicable, it can be assumed that these structures do not experience crosstalk unless stated otherwise. Therefore, when referring to a differential pair (or p-n, or skew-p and skew-n), it denotes two uncoupled traces used in a differential pair.

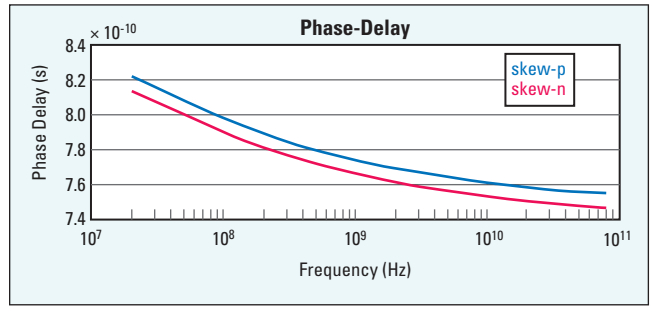

Fig. 5 **Frequency domain single-ended phase delay.**

With that clarification, it can be stated that one traditional and well-defined approach to measuring skew is in the frequency domain (see ***Figure 5***). To calculate skew, the phase delay is taken and the difference between them (skew) is computed, as illustrated in ***Figure 6***.

In Figure 6, two different skew responses are shown. In ***Figure 6a***, the skew is created using a single, flat delay across all frequencies; the delay remains constant at every frequency point. In ***Figure 6b***, the same delay is generated by adding extra length to one leg of the differential pair. In this case, the difference in length results in a frequency-dependent delay due to the dielectric constant varying with frequency; therefore, the delay also becomes frequency-dependent. This latter case results in higher skew-threshold sensitivities compared to the former flat-frequency response.

Frequency-dependent skew can arise from differences in transmission line lengths, such as bends or when the two members of a differential pair run over different dielectrics, which often occurs with reinforced fiber weave fabrics. When the delta length in the transmission line has a frequency-dependent dielectric constant (resulting in frequency-varying delay), the skew also becomes frequency-dependent, as shown in Figure 6b.

Regarding the advantages and disadvantages of this process, they can be summarized as follows:

Pros:

- Unambiguous definition: Each frequency arriving at the endpoint can be observed with a different delay.

Cons:

- Usage concerns: How can this information be effectively applied?
- Complexity for practical use: For example, is the skew at 100 MHz more significant than at 20 GHz?

- Communication challenges: A single number would be easier to convey for marketing purposes.

Some of the perceived challenges of this methodology can be addressed by performing measurements in the time domain.

Time Domain Definition

Skew is most commonly defined in the time domain by selecting a threshold and measuring the delay difference at that threshold, as illustrated in Figure 1. As previously mentioned, the primary drawback of this method is that the skew can vary based on the chosen threshold. This issue becomes more pronounced when the signals are not identical. For example, one line may experience slight discontinuities, the driver might be somewhat asymmetric, or the two lines in the differential pair may not be driven with the same rise time. Additionally, significant coupling between the lines can affect their shapes, as seen in Figure 1, where one line tends to influence the other.

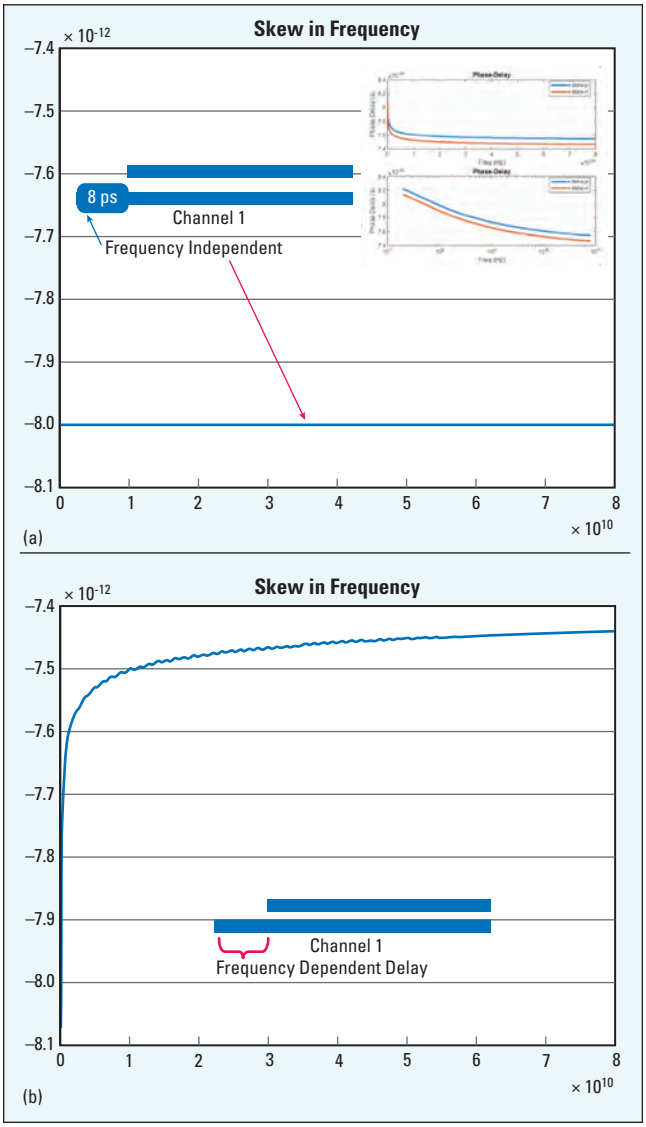

Fig. 6 **Frequency domain skew definition.**

To examine how skew variability is affected by the threshold, ***Figure 7*** shows a substantial difference in skew as the threshold changes. This variability raises the question: What is the true skew in this topology?

- Should the skew be defined using the 50% point of these waveforms?
- Alternatively, should the 10% point be selected to focus on capturing the true delay while minimizing the impact of variations in edge shape?

It is important to note that, as shown in Figure 7, the two signals appear quite similar in shape. In this case, the skew arises from two different-length single-ended transmission lines. With coupling, the signals influence each other, leading to differences in the shape of the positive and negative sides, which further complicates the threshold skew discrepancy.

If one were to categorize the advantages and disadvantages of this approach, they might say:

Pros:

- Simple, yielding a single number.

Cons:

- Ambiguous; the skew is dependent on the threshold, meaning any desired skew value can be provided based on the chosen threshold.

Both the time and frequency domain definitions of skew have their advantages and disadvantages, leading to a desire for a more clearly defined and easily measurable way to define skew. This prompts consideration of what is important for the receiver. To maximize what the receiver sees, an alternative approach known as the pulse correlation method will be introduced.

Pulse Correlation Skew Method

To illustrate this method, consider a simple example shown in ***Figure 8***. Imagine there are two drivers that exhibit slightly different rise times (3

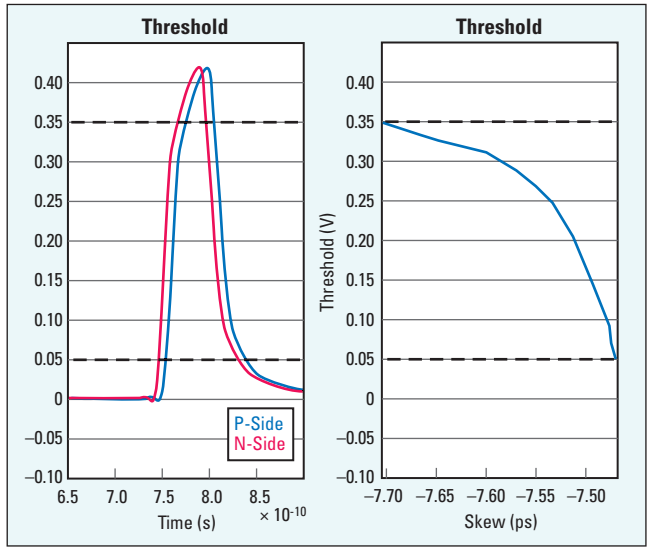

Fig. 7 **Time domain skew variation due to threshold.**

and 5). Additionally, there is a noticeable delay difference in the traces, which are assumed to be single-ended for simplicity (without coupling between them); one has a delay of 11, while the other has a delay of 13 (resulting in a -2 difference).

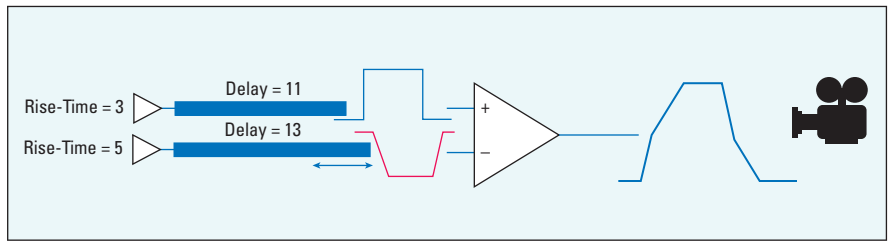

Fig. 8 **Skew seen at the receiver.**

It is important to note that delays are unitless; it does not matter whether they are measured in seconds, femtoseconds, or any other unit. For this example, the absolute values are not crucial, but it is essential that all delays are expressed in the same unit — whatever that may be — and that the relative differences between them are understood.

When observing the signal at the receiver, it becomes apparent that the differential signal appears distorted based on the phase delay delta of the transmission line and the differences in signal shape (represented here by the varying rise times, but it could relate to other factors as well). The unusual shape observed at the receiver can be readily explained by examining the two waveforms at the input of the differential receiver.

The question now being asked is: How much should one pulse signal be delayed relative to the another to maximize signal energy at the receiver?

One effective method for determining the optimal alignment between two pulses is to perform signal correlation and select the delay value at which the correlation is maximized. This correlation indicates the delay necessary to align one waveform with the other to achieve the highest energy at the receiver.

For instance, in Figure 8, with a bottom trace delay of 13, if skew is defined as the delay difference, one might conclude that a delay of -2 on the bottom trace (adjusting it to 11, equal to the top trace) would yield the best outcome. However, as demonstrated in ***Figure 9***, this assumption is flawed because the analysis did not account for the rise time difference; the asymmetry in the differential signal (DIFF) illustrates this point.

To achieve optimal energy alignment, the skew actually requires an additional -1. This means that for this receiver, the ideal scenario would involve a delay of 12 for the bottom trace, rather than the 11 shown in ***Figure 10***. Consequently, in this case, the correlation skew in the right figure is 0, and the differential signal perceived by the receiver exhibits significantly better symmetry.

By comparing the DIFF traces in Figures 9 and 10, it becomes evident that the symmetry of the skew-correlated waveform in Figure 10 is improved compared to that in Figure 9. This enhanced symmetry contributes to a more optimal eye opening at the receiver. Therefore, it is logical to measure

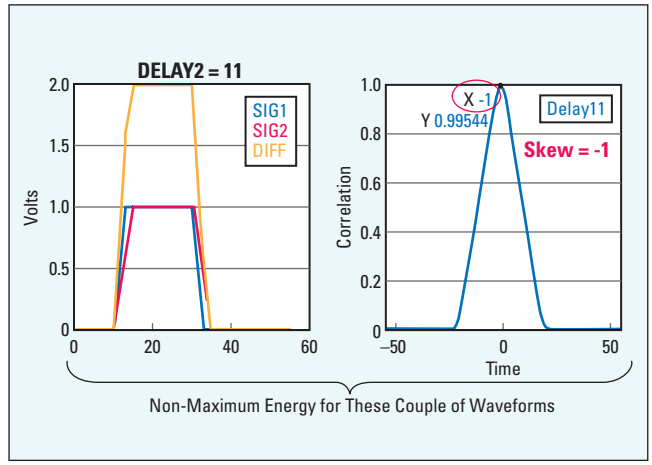

Fig. 9 **Correlation: non-maximum energy.**

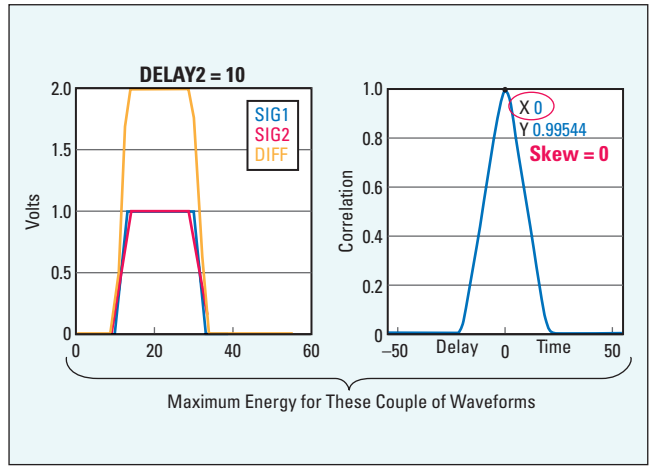

Fig. 10 **Correlation: maximum energy.**

skew in relation to this ideal symmetry.

This method also offers features that the traditional time domain edge skew method lacks. Notably, it is not dependent on a threshold (since no threshold is defined), but it is important to recognize that it has its drawbacks. Here is a summary of the pros and the cons of this method:

The Good:

- Threshold-independent; produces a single value
- Provides a straightforward and valuable metric due to its singular nature
- Represents the optimal intra-pair skew needed for the receiver to maximize energy
- Accounts for differences in trace shape.

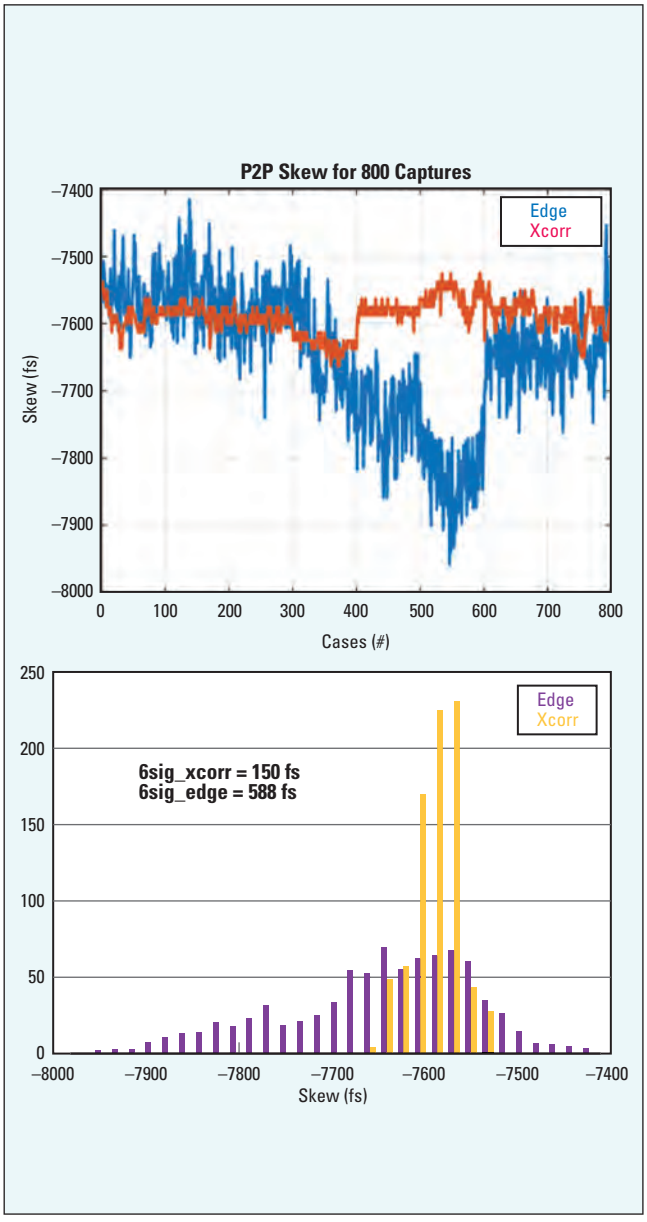

Fig. 11 **Time domain skew measurements.** ***Source:*** **Samtec Corporation.**

The Bad:

- Pulse width dependent; though it exhibits less variation compared to the edge threshold method, some dependency still exists
- The computation algorithm is somewhat more complex, and there are concerns about integrating deterministic distortion (such as reflections and ringing) on the pulse, particularly in reflective topologies.

Time Measurement Example

It would be valuable to evaluate the performance of both algorithms (the edge method and the correlation method) through real measurements using a time domain instrument. Conducting multiple measurements on a device under test could yield insights into the potential advantages and disadvantages of each approach.

Figure 11 illustrates the skew measurement for a coupled uniform differential pair using both the edge method and the correlation method. The measurement process is outlined as follows:

- **Edge Method:** A step signal is sent as a time domain reflectometry (TDR) signal. A threshold is set at the 50% point of the reflected waveform on each leg of the pair. The measured delay is divided by two (given that TDR readings represent double the actual physical delay), and skew is calculated by subtracting the delay between the two lines of the pair.
- **Correlation Method:** A step signal is also sent as a TDR. The incident and reflected impulse responses are generated by differentiating the step. A pulse response is then created by convolving these impulses with a 500 ps pulse. The two reflected pulses from each leg of the differential trace are correlated, and the resulting delay from the correlation is divided by two to obtain the skew.

By repeating these measurements 800 times, clear differences in sensitivity between the two methods can be observed, both in the track and in the histogram. Notably, the correlation method yields a more stable track and standard deviation for the skew measurement. Furthermore, the variation of skew due to pulse width appears to be significantly smaller with the correlation method compared to the edge threshold method; this aspect is outside the scope of this article.

Conclusion

In summary, as demonstrated in the equivalent channel example, intra-pair skew is a crucial metric when working with multiple lines. Its behavior, measurements, and interpretations are closely linked to other forms of signal degradation, making the definition of a single skew value a nuanced issue that requires careful consideration.

This work has introduced three distinct methods for measuring skew:

- Phase Delay vs. Frequency
- Time Domain Edge Threshold
- Time Domain Pulse Correlation

Each method presents its own advantages and disadvantages. It is important to recognize that when measuring very small skew values, noise and other factors can easily affect the results. Generally, edge methods are convenient and applicable in many situations, but they may provide lower resolution and sensitivity compared to correlation methods. If understanding delay differences at specific frequency ranges is a priority, the frequency method may be more suitable. Ultimately, the choice of measurement technique should be guided by the context and the specific goals of the skew measurement.

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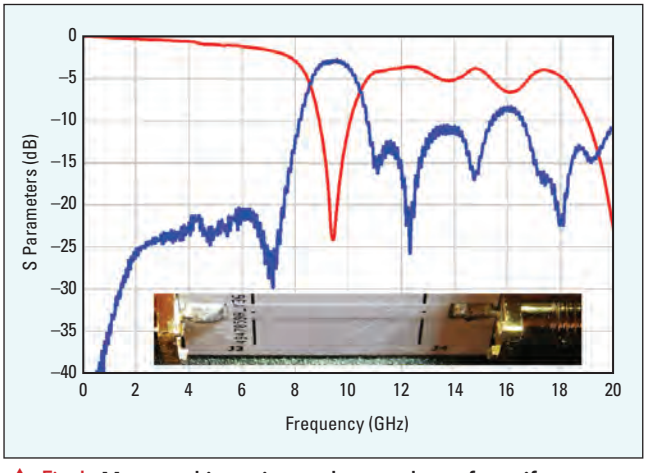
A Subtle Problem to Avoid in Your Next Design

Eric Bogatin, Technical Editor, Signal Integrity Journal
Dheeraj Gooty, University of Colorado Boulder

An expert is someone who has made all the mistakes possible. However, one does not have to have made all the mistakes firsthand, as long as one can learn from the mistakes of others.

A board recently built by a student showed a strange resonance, which took a bit of sleuthing to resolve. ***Figure 1*** provides an example of the return and insertion loss (IL) of a simple uniform transmission line, showing the sharp suck-out at about 9.4 GHz. This sort of sharp dip in IL and a corresponding peak in the return loss (RL) is a signature of a resonance. But where was the resonance coming from? It was just a simple, short transmission line.



▲ Fig. 1 **Measured insertion and return loss of a uniform transmission line, shown in the inset. Where is the resonance coming from?**

Now that the root cause of this anomaly is understood, it can be avoided. Here is the lesson that was learned.

What to Avoid During Design

This simple board was a 2-layer board, with a solid ground plane on the bottom layer. The SMA ground pins were soldered to the bottom of the ground plane and the signal pin was soldered to the top signal trace. This sort of suck-out in the IL is an indication of a resonance stub somewhere. But there were no vias on this board, and there were no routing stubs anywhere. What was resonating? It turned out to be a thermal relief feature in the ground pad of the SMA connector.

The purpose of the thermal relief is to aid in the assembly of the circuit board. A thermal relief structure creates a short isolation "moat" or a gap in the solid copper, with a few very short "bridges" that span the gap to provide an electrical connection. The moat provides thermal isolation, and the bridges provide electrical connection.

While a solid copper flood connection gives the best electrical performance, it also serves as a heat sink for pins connected to a plane. This sink will effectively pull the heat away from the pin during soldering and may produce poor solder joints in

the connection. A thermal relief structure for ground vias is important when soldering through-hole pins connecting to the ground plane.

When adding the pad to solder the SMA ground leads, the EDA tool, in its infinite wisdom, automatically adds a thermal relief structure. This structure, shown in ***Figure 2***, inadvertently introduced a signal integrity artifact. This is an example of the law of unintended consequences.

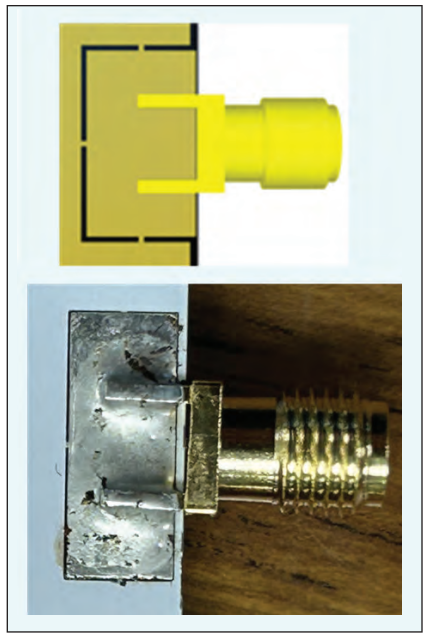


Fig. 2 **Examples of the thermal reliefs added to pads to make soldering more reliable.**

When a signal is launched into the SMA pin from an external source, the return current will cross this slot in the pad and induce a "slot wave mode" of current between the copper edges of the slot.

Once launched into the slot, the signal will propagate down the slot between the edges, to the short, narrow tabs (bridges) that look like an electrical short across the slot. The slot wave mode will rattle back and forth between the shorts, creating a resonance. Since the slot wave cavity has the same boundary conditions on both ends, the resonances arise when a multiple of half wavelengths can fit between the ends of the cavity. The first resonance frequency is roughly:

$$f0[GHz] = \frac{11.8}{2 * sqrt(\,Dk\_eff\,) * Slot\,Length[\,in.\,]} \quad (1)$$

The shorter the distance between the shorting tabs, the higher the resonant frequency. When the length is 0.5 in., the resonant frequency is about 6 GHz if the effective Dk is 4. There is an uncertainty related to the unknown Dk_eff when the dielectric is inhomogeneous, such as when the plane is a surface layer.

A Test Board

It is good practice in a lab to approach all problems with a three-tiered approach:

- Analyze the problem based on first principles to identify and understand the root cause
- Simulate the problem to verify that the effect can be turned on and off
- Design, build, and measure a test vehicle to demonstrate the best design practices to eliminate the problem and pathological practices that accentuate this problem.

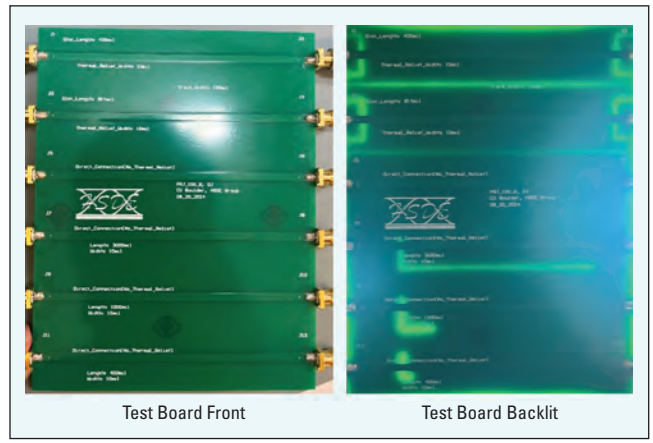


Fig. 3 **The test board displays the slots under the signal line when backlit.**

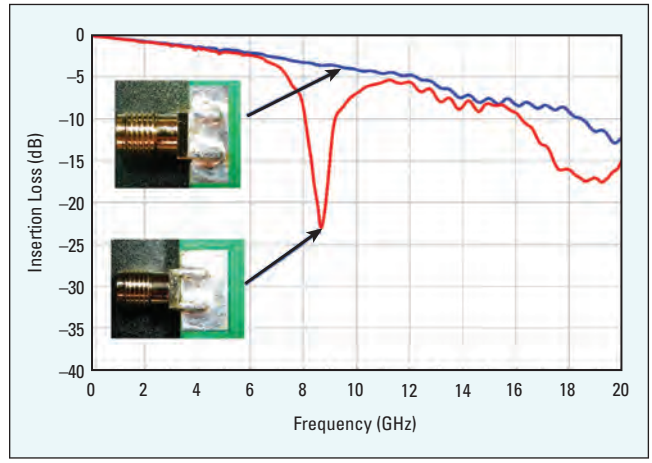


Fig. 4 **IL plot for the transmission lines, with and without thermal reliefs.**

The test board designed to explore the resonances from slots is divided into two sections. The upper half of the board had thermal relief slots in the return plane in the footprint of the launch. The bottom half of the board had no thermal relief slots at the launches, but had slots of various dimensions introduced beneath the trace. The slot wave mode in the slots was driven by the return currents of propagating signals. ***Figure 3*** shows the board and a few of the slots that were intentionally introduced.

Measurement Analysis

For an ideal PCB transmission line, the RL (S11) at low frequency should be a large negative dB value, and the IL (S21) should be 0 dB at low frequency. The IL will decrease with frequency due to losses. The presence of a slot to which the return current couples will suck out energy at the slot wave resonant frequency. This will also result in a higher impedance and a larger RL at the resonant frequency. The first example illustrates the ability to turn this

slot wave mode off and on.

Two identical 50 Ω test lines were constructed, one with the thermal relief slots in the SMA launch and one without the thermal relief. ***Figure 4*** shows the comparison of the IL of these two lines.

An important consistency test is to estimate the frequency at which one would expect the slot wave mode resonant frequency. Given its length of 0.4 in., and roughly estimating the effective Dk as 3.0, the expected resonant frequency is 8.51 GHz. This is remarkably close to what is measured, which is 8.6 GHz.

The combination of turning this effect off and on and estimating the magnitude is strong confirmation of the suspected root cause.

Additional Examples

This analysis suggests that any slot in the return plane that return current couples to will drive a slot wave mode and suck out energy in the IL. A few slots in the return plane under the signal line illustrate this. ***Figure 5*** shows a close-up of three of these structures and their measured IL. In these structures, the slot was made 30 mils wide. This increases the contribution from the air and decreases the effective dielectric constant compared to the thermal reliefs.

The measured IL of each slot clearly shows the suck-out at increasing frequency as the length is decreased.

Calculating the resonant frequency for each requires an estimate of the effective Dk. This is a combination of the bulk value and the contribution of the air in the slot wave mode. For this 59 mil-thick board and 30 mil-wide slot, a value of 2.4 gives a prediction of the resonant frequencies for all three slots that matches to better than 5%, as summarized in the ***Table 1***.

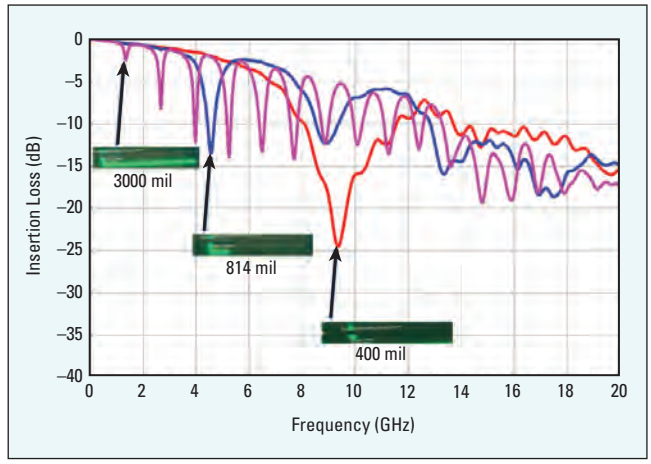
TABLE 1

	Estimated with Dk_eff = 2.4	*Measured*
400 mil slot	9.51 GHz	9.35 GHz
814 mil slot	4.67 GHz	4.56 GHz
3000 mil slot	1.26 GHz	1.34 GHz

Implications

This case study has pointed out one consequence of a signal passing over a slot in the return plane. A slot under one or more signal traces will generate the trifecta of noise. It will induce a slot wave resonance and suck energy out of the signal, and act as a discontinuity to create reflection noise. It will contribute to long-range cross talk to any other signal lines passing over this slot. And the slot wave mode signal will also act as an antenna and radiate.

This unexpected slot in the thermal relief pads



▲ Fig. 5 **Measured IL and a close-up of the slots introduced under the signal traces.**

was inadvertently added by the EDA tool. However, similar slots are also added to boards with split plane layers that are also used as return planes. This is why the best practice is to use solid return planes adjacent to all signal layers. If split power planes are used, do not use them as return planes.

One can estimate the resonant frequency of the slot wave mode as roughly 3 GHz/Length (in.) using a simple rule of thumb. If the slot is short enough, the resonant frequency can be pushed to a bandwidth well above the signal bandwidth in an application.

However, if it is a long slot, such as found in split power planes, it could create a resonance easily below 1 GHz, where many signal bandwidths lurk. Avoid making this mistake when designing a board.

Conclusion

Designing circuit boards is often like playing the whack-a-mole game. A change is made in one aspect of the design to fix a problem, only to have another problem pop up somewhere else. To reduce the problem of soldering on SMA connectors in an edge launch, a significant signal integrity problem has been introduced.

To reduce the problem of coupling to slot wave resonances, avoid using thermal reliefs in pads where the SMA is launched. However, if opting to use thermal reliefs, make sure the resonant frequency is well above the signal's bandwidth for the given application. Learn from this inadvertent mistake.

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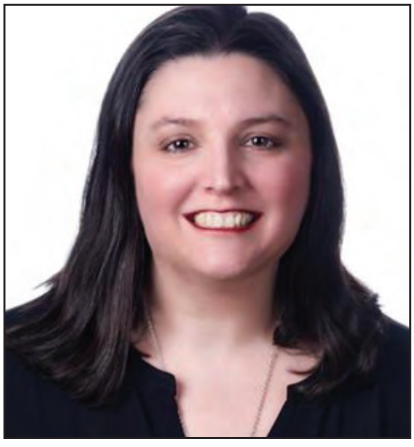

DesignCon gears up to celebrate its 30th anniversary this January with special events, an expo full of leading suppliers, and its highly regarded education.

Suzanne Deffree, Group Event Director, DesignCon

Between FedEx, UPS, and Amazon Prime, it's not unusual to find a package on my doorstep. But it's rare that I am as delighted as I was when recently opening a package from long-time DesignCon attendee, speaker, and Technical Program Committee (TPC) member Istvan Novak.

Istvan, a globally recognized engineer with Samtec, is known for giving back more engineering knowledge than can be measured across his decades of experience. In the package, he had shared a copy of the original DesignCon event handbook, full of technical papers and speaker information from the first show held in 1995.

This year at DesignCon, as part of our 30th Anniversary celebration, we will display that very same handbook that started it all. Taking place January 28-30, 2025, at the Santa Clara Convention Center, DesignCon will host a 30th Anniversary lounge on the expo floor with a QR code to download and save the handbook. Serving as a time capsule of the history of the event, with designs and papers that laid the groundwork for today's innovations, the handbook holds many contributions of people like Istvan, who have continued to share their insights with the design community over the past three decades.

Our 30th Anniversary celebration also includes a special Welcome Reception to mark the milestone, giveaway prizes, and a timeline wall located in the lounge space that will highlight some of the most important events and technologies over the past 30 years. There will also be a space on the timeline to predict the next big innovations, where we welcome guests to imagine what is to come for design manufacturing.

As DesignCon has for many years, the event will host a stellar education program vetted by our 99-member TPC, daily networking opportunities, and more than 170 exhibitors.

Education Highlights

While DesignCon 2024 attendee interest in optimizing high-speed link design remained strong, education in power integrity in power distribution networks, power supplies, and power delivery boasted the highest attendance. DesignCon's TPC advises that the impressive interest in power integrity stems from the increase in the power usage

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of new semiconductor devices and the booming of data centers, HPC, and AI/ML processors. This increased usage brings new effects in a PDN that negatively impact the product's performance and cause failures. Solving these problems requires new methods, new tools, and new approaches to develop PDNs for modern semiconductor devices.

Areas that showed the highest number of paper submissions for the 2025 conference (a good indicator of research activity and overall interest) were the core topics of modeling, analysis, and the optimization of interconnects and high-speed link design.

The following is a sample of the sessions rated highest by our TPC peer reviewers, with papers written and presented exclusively at DesignCon 2025:

"Balancing Current Density to High-Power ASICs in Lateral Power Delivery Designs" from Hewlett Packard engineers covers new via construction and optimization strategies.

"Statistical Modeling of System Power Integrity in Adaptive Embedded SoC for Artificial Intelligent (AI) Computing" comes from AMD engineers and examines efficient ways of modelling current consumption to help design for the increasing complexities of PDN and reducing over-design.

"Next Generation 224 Gbps-PAM4 Chip-to-Chip/MR SERDES, Package, Channels & Link Simulation & Analysis" from Intel engineers provides a thorough study on 224G analysis with an eye toward understanding design sensitivities and optimizing link operating characteristics.

"200-Gbps Lanes Equalization Methods & Required Fixture Bandwidth, S-parameter Bandwidth & Acquired Signal Bandwidth" comes from Tektronix engineers and covers the important topic of MLSD becoming a part of the link equalization.

"Via Design for 112 Gbps & Beyond: Theory & Reality" is a combined effort of Simberian and Intel engineers on how to deal with real-life problems such as manufacturing variations and tolerances, as well as the importance of EM field localization to close the gap between simulation and reality measurements.

Additional Education of Interest

- "Prediction of Dielectric Constant & Copper Roughness Parameters of High-Speed Automotive PCB Digital Interconnects Using a Data-Based Model" from the University of New Brunswick Fredericton and Institut für Theoretische Elektrotechnik
- "Tutorial – Power Delivery Network Master Class on 2000A: How to Design, Simulate & Validate" from Keysight, Broadcom, Signal Edge Solutions, and Picotest engineers
- "Reduced Order Geometric Macro Model of PCB Fiberglass Spatial Variation for Skew & Impedance Prediction" from Samtec engineers
- "Obtaining Accurate Signal Measurements: Active Probing" from Northrop Grumman engineers
- "Panel – The Expanded Role of SI/PI in Next Gen AI Data Center Development" moderated by Tektronix.

Further Information

In total, DesignCon 2025 is offering more than 160 educational sessions. Conference passholders will have access to the 14 tracks of education, plus the Drive World automotive-focused conference. All attendees have access to keynotes, panels, Chiphead Theater presentations, exhibitor-led education, the Engineer of the Year and Best Paper Awards presentations, and the DesignCon expo floor.

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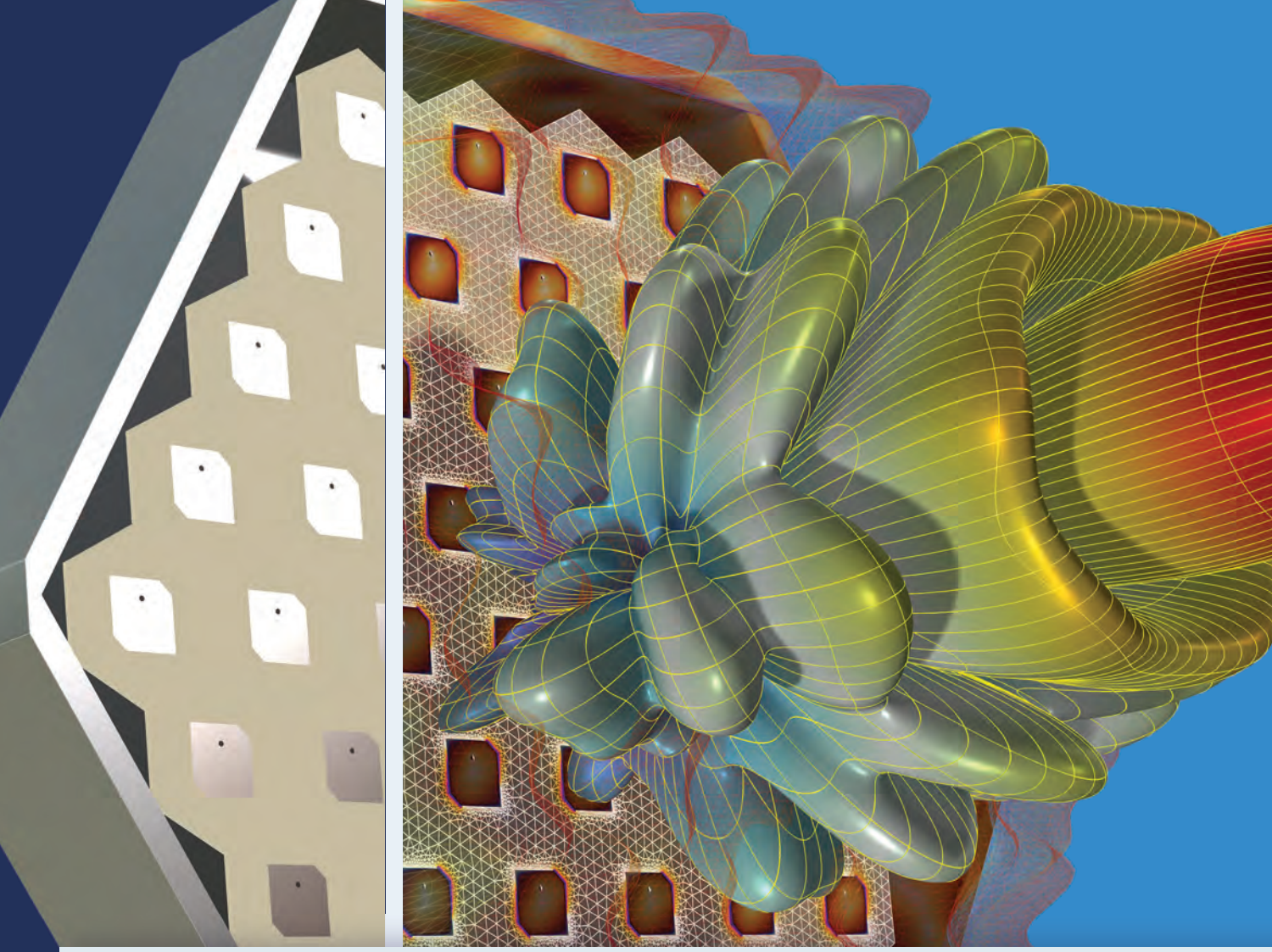

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