ISSN: 1863-5598

ZKZ 64717
02-26

Bodo´s Power Systems®

Electronics in Motion and Conversion

February 2026

Multiphysics Simulation and Simulation Apps in Power Electronics

COMSOL

PULSED INDUCTANCE MEASUREMENT

POWER CHOKE TESTER DPG10/20 SERIES

Inductance measurement from 0.1 A to 10 kA

KEY FEATURES

Measurement of the

- **Differential inductance** $L_{diff}(i)$ and $L_{diff}(\int Udt)$
- **Amplitude inductance** $L_{amp}(i)$ and $L_{amp}(\int Udt)$
- **Flux linkage** $\psi(i)$
- **Magnetic co-energy** $W_{co}(i)$
- **Flux density** B(i)
- **DC resistance**

Also suitable for 3-phase inductors

APPLICATIONS

Suitable for all inductive components from **small SMD inductors** to **very large power reactors in the MVA range**

- **Development, research** and **quality inspection**
- **Routine tests** of small batch series and mass production

KEY BENEFITS

- Very **easy and fast** measurement
- **Lightweight, small and affordable price-point** despite of the high measuring current up to 10000A
- **High sample rate and very wide pulse width range** => suitable for all core materials

AVAILABLE MODELS

Model	max. test current	max. pulse energy
DPG10-100B	0.1 to 100A	1350J
DPG10-1000B	1 to 1000A	1350J
DPG10-2000B	2 to 2000A	1350J *new model*
DPG10-2000B/E	2 to 2000A	2750J *new model*
DPG10-3000B/E	3 to 3000A	2750J
DPG10-4000B/F	4 to 4000A	8000J
DPG20-10000B/G	10 to 10000A	15000J

Technological leader in pulsed inductance measurement for 20 years

www.ed-k.de

Content

Supporters & Friends

A Media
Katzbek 17a
24235 Laboe, Germany
Phone: +49 4343 42 17 90
Fax: +49 4343 42 17 89
info@bodospower.com
www.bodospower.com

Founder
Bodo Arlt, Dipl.-Ing.
bodo@bodospower.com

Editor in Chief
Alfred Vollmer, Dipl.-Ing.
alfred@bodospower.com

Correspondent Editor Bavaria
Roland R. Ackermann, Dipl.-Ing.
roland@bodospower.com

Editor China
Min Xu – xumin@i2imedia.net

US Support
Rusty Dodge
rusty@eetech.com

Creative Direction & Production
Bianka Gehlert
b.gehlert@t-online.de

Publisher
Holger Moscheik
holger@bodospower.com

Free Subscription to qualified readers
Bodo´s Power Systems is available for the following subscription charges:
Annual charge (12 issues) is
150 € world wide · Single issue is 18 €
subscription@bodospower.com

Printing by:
Dierichs Druck+Media
GmbH & Co. KG
34121 Kassel, Germany

The Power of Physical AI

For over 10 years – except during the Covid Pandemic – I have always started my business year by attending the CES show in Las Vegas. Even though I am not a big fan of this city, I decided to fly to the desert because CES always gives me a glimpse of what to expect in the coming year. And so it was this year.

When I met Jochen Hanebeck, CEO of Infineon, at CES 2026 he said "the show is about AI everywhere". As his company now makes about 1.5 billion US-$ of annual revenue in the power business he didn't just speak about the "data flow" but he also added "do not forget the power flow!", and he is right.

We all know that server farms, which are needed for Virtual AI assistants like ChatGPT, Copilot or Gemini, consume a lot of power, but at CES the topic was more on "Physical AI", which means artificial intelligence systems embedded in or controlling physical entities such as robots, drones or autonomous vehicles. In short, Physical AI acts in the real world, while Virtual AI operates in the digital realm. Physical AI, in some applications also called "Edge AI", is just at the beginning, but it will definitely need a lot of efficient power solutions.

For quite a while, Alex Lidow, CEO of EPC, has actively emphasized the importance of efficient power solutions for robots, but this had felt more of a kind of niche market for me. However, at CES 2026 I had a very impressive demonstration of where robot technology will be going. Hyundai Motor Company, who acquired Boston Dynamics recently, showed its humanoid robot dubbed "Atlas", which is said to play a major role in the so-called software-defined factory (SDF). Humanoid robots will most likely have an exponential growth because they are so versatile. By 2028 Atlas is expected to perform high-precision sequencing activities, and by 2030 Atlas is promised to perform highly complex assembly tasks. Once some safety- and AI-related challenges are overcome, Atlas is scheduled to enter home applications like elderly care by about 2035.

After watching the video in my recent CES post on LinkedIn you will understand why I consider this a booming future market – especially when you consider that Atlas even did a somersault from a standing position. All these robots need power (and power control) stages for their actors (motors) as well as for their artificial intelligence functionalities. For me this simply means: There is something really big coming towards us.

Bodo's magazine is delivered by postal service to all places in the world. It is the only magazine that spreads technical information on power electronics globally. We have EETech as a partner serving our clients in North America. If you speak the language, or just want to have a look, don't miss our Chinese version at bodospowerchina.com. An archive, of every issue of the magazine, is available for free at our website bodospower.com.

My Green Tip of the Month:
Be more sustainable and avoid disposable cups, forks, knives, plates etc. by choosing reusable items. Having returned from the US to Central Europe I once again realized that it is so easy to avoid giant amounts of rubbish which – in the best case – still only get "thermally recycled" (the waste management term for "burned").

Alfred Vollmer

Events

The Magnetics Show Europe 2026
Amsterdam, NL February 24 – 26
https://themagneticsshow.materialsweekeurope.com

DesignCon 2026
Santa Clara, CA, USA February 24 – 26
www.designcon.com

PLECS Conference 2026
Zurich, Switzerland March 3 – 4
www.plexim.com

embedded world 2026
Nuremberg, Germany March 10 – 12
www.embedded-world.de

CIPS 2026
Dresden, Germany March 10 – 12
www.cips.eu

AMPER 2026
Brno, Czech Republic March 17 – 19
www.bvv.cz/en/amper

APEC 2026
San Antonio, TX, USA March 22 – 26
www.apec-conf.org

emv 2026
Cologne, Germany March 24 – 26
https://emv.mesago.com

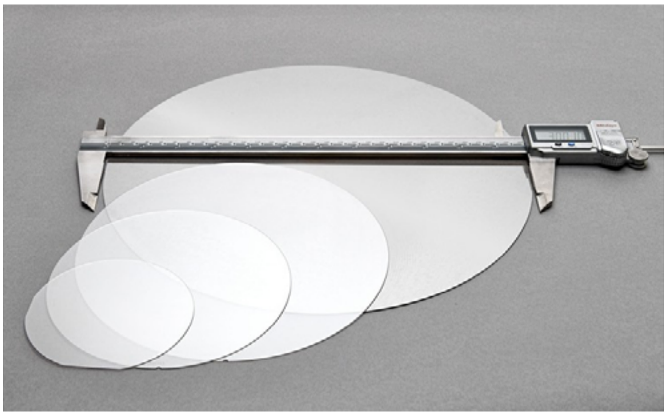
SEMICON China 2026
Shanghai, China March 25 – 27
www.semiconchina.org

300mm Silicon Carbide (SiC) Technology

Wolfspeed announced a significant industry milestone with the successful production of a single crystal 300mm (12-inch) silicon carbide wafer. Backed by its silicon carbide IP portfolios, comprising more than 2,300 issued and pending patents worldwide, Wolfspeed is pioneering the transition to 300mm technology, establishing a clear path to future volume commercialization.

This technology advancement represents a major step forward for next-generation computing platforms, immersive AR/VR systems, and high-efficiency, advanced power devices. By expanding silicon carbide to 300mm, Wolfspeed is unlocking new performance thresholds and manufacturing scalability for some of the world's most demanding semiconductor applications.

"Producing a 300mm single crystal silicon carbide wafer is a significant technology achievement and the result of years of focused innovation in crystal growth, boule and wafer processing," said Wolfspeed Chief Technology Officer Elif Balkas. "It positions Wolfspeed to support the industry's most transformative technologies, especially critical elements of the AI ecosystem, immersive augmented and virtual reality systems, and other advanced power device applications."



Wolfspeed's 300mm platform will unify high-volume silicon carbide manufacturing for power electronics with advanced capabilities in high-purity semi-insulating substrates used in optical and RF systems. This convergence will support a new class of wafer-scale integration across optical, photonic, thermal, and power domains.

www.wolfspeed.com

Co-Development on SMPS Solutions for AI Server Power Supplies in Korea

The French company Wise Integration and the Korean companies Powernet and KEC have signed a strategic memorandum of understanding (MoU) to co-develop next-generation switched-mode power supply (SMPS) solutions designed specifically for AI server applications in South Korea. The partnership aligns with the country's push to expand AI infrastructure and build out the next generation of high-density data centers. Under the agreement, Wise Integration will supply its GaN power devices, digital-control expertise and technical support. Powernet Technologies will lead the development of SMPS designs using Wise's WiseGan® and WiseWare® technologies. KEC Corporation will manage backend manufacturing, including module integration and system-in-package production tailored to the thermal and reliability demands of AI-server racks. The collaboration builds on an earlier partnership between Wise Integration and Powernet, launched to serve OEMs that require compact, digitally controlled power-supply systems for faster, smaller and more energy-efficient electronic equipment.

www.wise-integration.com

Fabio Necco Appointed as CEO

Cambridge GaN Devices (CGD) announced the appointment of Fabio Necco as Chief Executive Officer. The move is designed to drive forward CGD's entry into key markets. Necco takes over as CEO from CGD Co-founder, Giorgia Longobardi, who made the announcement, saying, "I am delighted to welcome Fabio to CGD and hand over the day-to-day leadership of the company while I channel my energy into my passion for bringing advanced, sustainable and energy-efficient power electronics solutions to market. Fabio, is the right person with the right skill set to take CGD into its next growth phase, and I shall do all I can to support his initiatives as I transition into my new role as CMO at CGD."

Necco comes to CGD from onsemi, where he was vice president and division general manager with more than 25 years' experience in power electronics, application engineering, vehicle electrification, and data centres, all primary market focus points of CGD. Necco said, "CGD is at an exciting juncture in its history. I have known CGD and Giorgia for years and have long been impressed with its success under her leadership. I am very excited about CGD's unique technology and to have been chosen to lead our entire team to the next stages of product development as well as substantially increasing our presence in key markets."

www.camgandevices.com


ROHM
SEMICONDUCTOR
EcoSiC
Meeting your needs. Portfolio expansion.
SiC Power Modules
HSDIP20
DOT-247
TRCDRIVE pack™
Case type
C type
E type
G type
● Compact 4-in-1/6-in-1
● Circuit-oriented element layout (4-in-1, 2-in-1, etc.)
● Improved heat dissipation characteristics
● 2-in-1 TO-247-4L
● Improved heat dissipation performance
● Half-bridge/source common
● Parallel multi-chip configuration provides high current capability
● Low Ls improves switching performance
● Reduced size through improved heat dissipation performance
● Parallel multi-chip configuration provides high current capability
● Gel encapsulation in case
TRCDRIVE pack™ and EcoSiC™ are trademarks or registered trademarks of ROHM Co., Ltd.
www.rohm.com

MEMS-Based Hot-Switched Power Panel Validated

Menlo Microsystems announced in partnership with Microchip Technology that it has successfully completed the hot switching validation of a MEMS-based 1000V/500A (0.5 megawatt) relay panel that is the basis platform for future development of advanced circuit protection systems for the U.S. Navy.

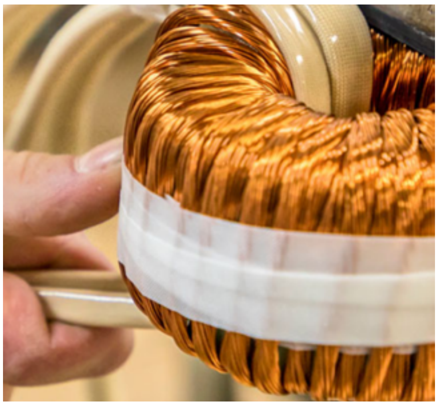
This accomplishment marks the first-ever validation of a MEMS-based 0.5 megawatt hot-switched relay panel for naval applications in the United States and is a critical step in the Navy's 10-megawatt Advanced Circuit Breaker program.

Menlo Micro has successfully advanced through the program's multiple phases of advancing complexity demonstrating the performance and scalability of its Ideal Switch® technology for power applications. Validation testing of the latest phase was completed at Microchip Technology's advanced power test facilities.

www.menlomicro.com

Strategic Move extends Electronics Portfolio and Industry Production Footprint in EU

ITG Electronics has acquired Max Holzinger & Co GmbH, a Germany-based manufacturer of high-reliability components for a variety of industries. The acquisition marks a significant milestone in ITG's long-term strategy to expand its European manufacturing footprint and strengthen regional supply capabilities. Under the new structure, MH will operate as an independent entity formally folded under ITG Deutschland GmbH, ITG Electronics' European division. It will also carry the designation of a Member of ITG Companies, reinforcing its integration within ITG's global family while maintaining its established identity, expertise, and customer relationships. The acquisition represents ITG's continued European manufacturing investment, reflecting a strategic shift toward regionalized production. In 2015, ITG diversified manufacturing into Vietnam as part of a country-risk reduction initiative. A decade later, ITG is continuing this evolution by expanding its capabilities into Europe, bringing manufacturing closer to key customers across the continent and bolstering resilience through geographic diversity.



"We are proud to welcome Max Holzinger & Co GmbH into the ITG family," said Martin Kuo, Director of Future at ITG Electronics. "This acquisition not only enhances our high-reliability and manufacturing capabilities, but also aligns with our long-term vision of regionalized production. With a trusted manufacturing partner based in Germany, we can better serve European customers who require precision, durability, and expedient support."

www.itg-electronics.com

Manufacturing Collaboration and Business Partnership in India

ROHM and Tata Electronics announced that they have entered into a strategic partnership for semiconductor manufacturing in India for both Indian and global markets. This partnership aims to leverage the expertise and ecosystem of both the companies in order to expand business opportunities for both ROHM and Tata Electronics, thereby further strengthening the relationship between the semiconductor industries of Japan and India.

As an initial focus, ROHM and Tata Electronics will establish a manufacturing framework for power semiconductors in India by combining ROHM's leading device technologies with the advanced backend technologies of Tata Electronics. In addition, by integrating the sales channels and networks, the partnership will create new business opportunities in the Indian market and deliver higher-value solutions to a wide range of customers. As the first step in this collaboration, Tata Electronics will assemble and test ROHM's India-designed automotive-grade Nch 100V, 300A Si MOSFET in a TOLL package, targeting mass production shipments by next year.

The companies will also explore co-development of high-value packaging technologies in the future. Both companies will combine efforts to market the products manufactured through this collaboration.

www.rohm.com

Michael Budde elected President of ESIA

The General Assembly of the European Semiconductor Industry Association (ESIA) has elected Michael Budde, President Mobility Electronics at Bosch, as the organisation's new President for the next two years. ESIA represents and promotes the common interests of the Europe-based semiconductor industry towards the European institutions and stakeholders. Mr Budde is succeeding Infineon Technologies' CEO Jochen Hanebeck.

Michael Budde has served as divisional chief executive since October 2022. His career within Bosch spans over two-and-a-half decades of leadership experience and garnered him comprehensive expertise of the automotive industry. Mr Budde had gathered insights in electrical drives, battery systems, and various sales & marketing roles, including an international assignment in the United States. Under his guidance, Bosch has strengthened its position in semiconductor-based solutions for consumer and mobility applications, leveraging his deep understanding in the automotive industry and a close collaboration with OEMs. He holds a degree in mechanical engineering from the Rheinische Fachhochschule (RFH) in Cologne, Germany.

www.eusemiconductors.eu

Power Management Resource Center

Mouser Electronics announces its comprehensive power management resource center. With the proliferation of compact, high-performance, and battery-operated devices, power management design is critical to achieving optimal performance. By leveraging new advancements in power management, such as smart grid management technology, DC microgrids can enhance energy efficiency and power quality. Their native DC architecture provides seamless integration with DC loads and renewable energy systems, such as EV charging infrastructure. Another method of power management is energy harvesting, where improved conversion efficiency in solar, motion, and thermal harvesting techniques extends battery life or even enables completely battery-free operation.

For chip-level power and performance, modern embedded systems today utilize configurable logic blocks (CLBs). CLBs enable hardware-based functions, such as timing control and power sequencing, resulting in faster response times, reduced CPU load, and lower power consumption. Together, these advancements create a balanced system where power is generated, distributed, and consumed with maximum efficiency, fundamentally improving power management in electronics.

Mouser's technical team and trusted manufacturing partners tailor the resource center content to provide a trusted source of articles, blogs, eBooks, and new products from top manufacturers for power management. The hub also offers infographics on battery energy storage systems (BESS), helping professionals understand the system complexities and how to select the best-suited components. For engineers looking to stay ahead of the accelerating pace of advanced power management, the resource center serves as a valuable resource.

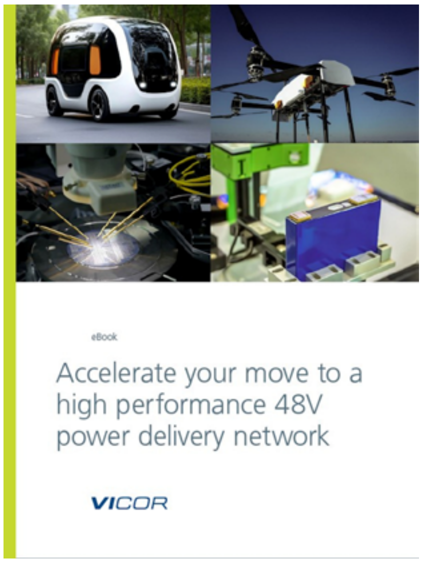
www.mouser.com

eBook provides Guidance on Designing 48V Power Delivery Networks

Vicor has published "Accelerate your move to a high-performance 48V power delivery network", a new 34-page eBook. This resource provides engineers and system designers with helpful tips and concepts to consider to transition from 12V power delivery networks (PDNs) to 48V. This free in-depth guide will help optimize power delivery to gain a competitive edge in the market.

Today computing, automotive, and industrial applications demand higher performance and efficiency and traditional 12V architectures are reaching their limits. Higher performing 48V architectures that reduce I2R losses are emerging as the obvious solution which not only unlocks power system capabilities, it also enables new levels of innovation.

Filled with useful insights and real-life applications, the informative eBook provides expert guidance on designing 48V power delivery networks to enhance the performance, efficiency and reliability of industrial products. Engineers can learn how the 48V PDN evolved, how to overcome power design challenges and how others have implemented successful power delivery networks that deliver competitive advantage. Readers can also learn how to leverage high-performance power modules to quickly prototype and implement a 48V PDN.



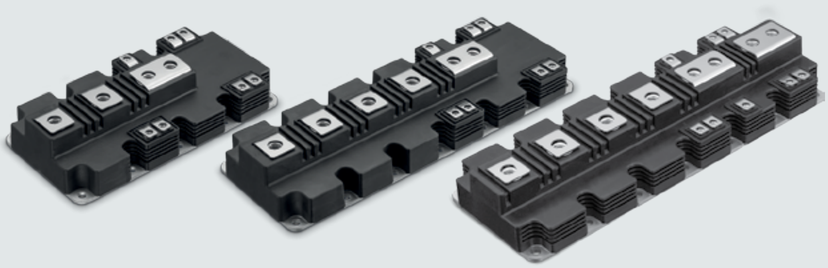
"With the rapid growth of AI and the infusion of higher voltage electrification, power delivery can provide a competitive advantage," said David Krakauer, VP of Marketing, Vicor. "This eBook explores why 48V distribution is quickly becoming the standard for next-generation designs, delivering benefits such as reduced conduction losses, improved thermal performance and smaller, lighter power delivery networks. This eBook offers the insights you need to accelerate your transition from 12V to 48V."

www.vicorpower.com

Fuji Electric
Innovating Energy Technology

PrimePACK™ 7G IGBT Modules

Upgrading to 1200 A/1200 V in PP2, 2400 A/1200 V & 2400 A/1700 V in PP3+ with RC-Technology



MAIN FEATURES

- Newly developed 7G IGBT, FWD & RC-IGBT
- Improved solder material for higher reliability
- Higher lifetime at same ΔT*j*
- Increased output power
- Lower conducting and switching losses
- 2nd label with $V_{CE(sat)}$ and V_F classification for easier paralleling

MV-INV

SOLAR

WIND

www.fujielectric-europe.com

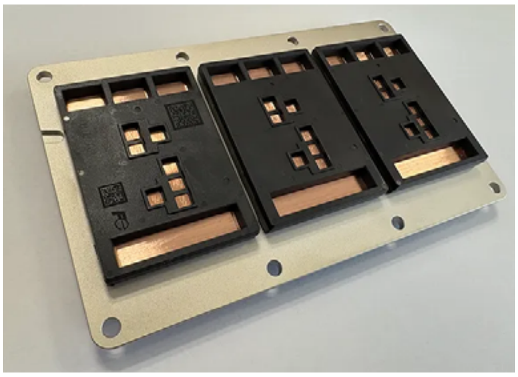
Chris Jacobs named Senior Vice President, Marketing and Product Strategy

Power Integrations announced the appointment of Chris Jacobs as senior vice president for marketing and product strategy. Mr. Jacobs brings a wealth of experience in the semiconductor industry, with an outstanding record of product execution, customer acquisition and strategy development across a range of end markets. He joins Power Integrations from Micron Technology, where he served most recently as vice president and general manager for the automotive, industrial/multi-market and consumer market segments of the company's multi-billion-dollar automotive & embedded business unit. Previously, Mr. Jacobs spent more than 25 years at Analog Devices, holding a succession of leadership roles including vice president for marketing and business development in the company's power IC and module business and vice president and general manager for the autonomous transportation & automotive safety business unit. He holds an MBA from Boston College, an MS in electrical engineering from Northeastern University and a BS in computer engineering from Clarkson University. He has also completed executive leadership programs at Stanford University and MIT.

www.power.com

Collaboration on SiC Power Semiconductor Modules with Mechanical Compatibility

Fuji Electric announced an agreement with Bosch to collaborate on SiC power semiconductor modules for electric vehicles that feature package compatibility.



By flexibly modifying the size and number of mounted chips, these modules can accommodate a wide range of power requirements and OEM circuit configurations. Moving forward, both companies intend to develop SiC power semiconductor modules with mechanical compatibility in terms of package outer dimensions and terminal positions. This will enable either module to be integrated into an inverter system without additional mechanical modifications, thereby minimizing the adjustment effort required for customers when using both module options in their systems. This collaboration aims to shorten design periods and contribute to diversifying procurement sources. As a result, engineers will be able to use SiC power semiconductor modules from both companies without altering their inverter system specifications, leading to reduced design time and diversified procurement. Furthermore, both companies plan to jointly develop user application technologies related to cooler design and various terminal connections when integrating SiC power semiconductor modules into inverter systems, and plan to provide technical support to customers.

www.fujielectric.com

Power Semiconductors: Global Distribution Network

Navitas Semiconductor has expanded its distribution agreement with Avnet, making Avnet a globally franchised strategic distribution partner for Navitas. The deal is part of the ongoing consolidation of Navitas' franchised distribution partners. Under the terms of the partnership, Avnet will supply technical and commercial expertise for Navitas' GaN and SiC, high-voltage and high-power wide bandgap semiconductor devices. This will better support the growth of AI data centers, high performance computing, renewable energy, grid infrastructure, and industrial electrification.

www.navitassemi.com

Strategic Collaboration of Automotive Tier-1 Supplier and Semiconductor Manufacturer

onsemi extended its strategic engagement with FORVIA HELLA with the adoption of onsemi's PowerTrench® T10 MOSFET technology across its automotive platforms. onsemi's PowerTrench T10 MOSFET technology delivers high efficiency with low conduction and switching losses, enabling high power density in a compact footprint. The collaboration is expected to "deliver smarter automotive power solutions with superior efficiency and optimized performance".

www.onsemi.com

Japanese precision since 1935

HIOKI

High-accuracy **Power Analyzers** & **Current Sensors** from a single source.

- Unrivalled accuracy at high frequencies
- Current Sensors from 2 A to 2000 A
- Max. 15 MHz sampling rate
- Up to 5 kV / 4 MHz

Discover more online!

HIOKI EUROPE GmbH
Helfmann-Park 2
65760 Eschborn
hioki@hioki.eu

shop.hioki.eu/PW8001

PSMA Magnetics Committee and PELS TC2 High Frequency Magnetics Workshop

The PSMA Magnetics Committee and IEEE PELS are currently planning to conduct the eleventh Power Magnetics at High Frequency Workshop on Saturday, March 21, 2026, which is the day before and at the same venue as APEC 2026 in San Antonio, TX. The 2026 workshop will build on the ongoing dialogue generated throughout the first ten workshops.

The purpose of this workshop is to explore recent improvements in magnetic materials, coil (winding) design, construction, and fabrication, as well as evaluation techniques, characterization methods, and modelling and simulation tools. The workshop targets the advancements deemed necessary by the participants for power magnetics to meet the technical expectations and requirements of new market applications where higher operating frequencies and emerging topologies are driven by continuous advances in circuits topologies and semi-conductor devices.

The target audiences for the 2026 Power Magnetics @ High Frequency workshop include the designers of power magnetic components for use in electronic power converters, those who are responsible to implement the most technologically advanced power magnetic components necessary to achieve higher power densities, specific physical aspect ratios such as low profile, higher power efficiencies and improved thermal performance. The target audience also includes people involved in the supply chain for the power magnetics industry ranging from manufacturers of magnetic materials and magnetic structures, fabricators of magnetic components, providers of modelling and simulation software as well as manufacturers of test and characterization equipment.

The theme of the 2026 Power Magnetics @ High Frequency is measurements and data processing trends to improve analytic models and simulation models towards developing better design tools, enabling magnetics optimization for existing and emerging applications. The workshop will address various aspects of measurement methods and creation of analytical models employing equations re-enforced with empirical data.

The workshop will open with a keynote presentation by Peter Zacharius of the University of Kassel, reviewing the basic principles of analytical models for magnetic components. During the morning session Lukas Pniak of Safron Research and Technology Center will present models for capacitive coupling of planar transformers, Miroslav Vasic of the Universidad Politécnica de Madrid will discuss Artificial Neural Networks and Digital Twin to optimize the design Dual Active Bridge transformers, Alfonso Martinez of Würth Elektronik will address modelling of stray capacitance and leakage inductance. Marek Rylko of SMA Magnetics will finish the session by reviewing the Scientific Network – Magnetics' project comparing core loss measurements using different measurement techniques.

During lunch, breakfast, and the networking hour at the end of the workshop there will be an interactive session of tabletop technology demonstrations, each addressing specific technical disciplines and capabilities consistent with the workshop agenda. Workshop attendees typically spend ten to fifteen minutes at each technology demonstration station viewing informal interactive presentations. The technology demonstration format facilitates Interaction between the attendees and the presenters as a segue from the morning technical presentation sessions to the afternoon lecture presentation session. Technology demonstrations are confirmed by Mike Arasim of Fair Rite covering magnetic core geometries for modern power applications, Ihsan Dalgic of Hioki addressing measurement equipment for magnetic components, Tobias Trupp of Magnetec collaborating with JC Sun of Bs&T covering the topic of apparent permeability and quality factor, Lukas Mueller of Micrometals collaborating with Jacob Lamphere of the University of Nebraska addressing current driven methods for characterization of core loss, Kevin Hermanns of PE Systems covering testing and modelling of magnetic components, Sebastian Bachman of Tridelta collaborating with Fritz Wohlrath of STS and Lucas Riebenweber of Coburg University introducing a new generation of magnetic cores, Joaquim Tristan of University of Pittsburgh addressing automated methods for characterization of magnetic core loss, Marcin Kacki of Hitachi Energy collaborating with Lufan Zhou of Universidad Politécnica de Madrid, Jun Wang of the University of Bristol covering triple pulse testing of magnetic cores and components, David Ruiz Gomez of Würth Elektronik introducing test methods to validate the voltage rating of magnetic components and Alfonso Martinez of Würth Elektronik introducing the CoreDataX database.

There is room for additional technology demonstrations. If anyone is interested to present a technology demonstration, they are encouraged to contact the workshop organizing committee via e-mail to power@psma.com .

The afternoon session will begin with a keynote presentation by Asier Arruti Romero of Mondragon University focusing on the development of unified magnetic loss model bridging empirical equations and physical insight. The keynote presentation will be followed by lecture presentations by Reddy Andapally Bharawaj of CBMM addressing data collection and analysis to create accurate models for FEA simulations, Andrija Stupar of SIMPLIS Technologies speaking to the development of magnetic models for power electronics simulation and Chema Molina of Frenetic providing insights to artificial intelligence-driven approaches for the design of magnetic components.

Registration for the workshop is limited and is open at the following URL: https://psma.com/node/8068

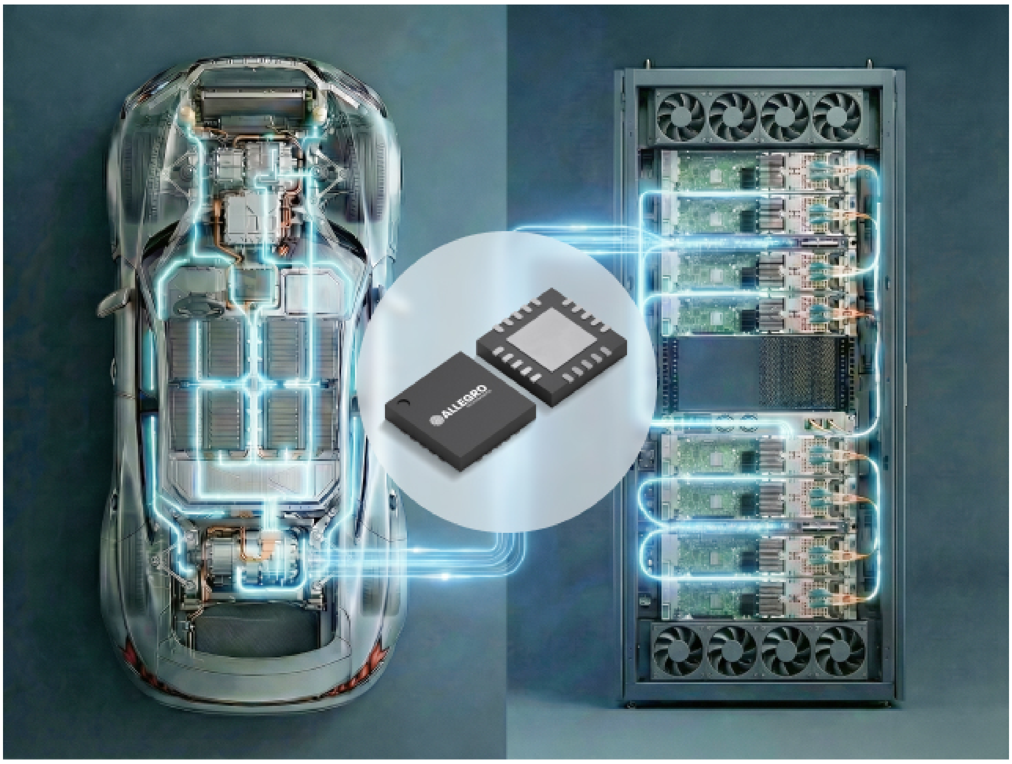
Any company interested in financially supporting the workshop as a partner can find more information regarding partner opportunities and benefits at the following URL: https://psma.com/node/8076

Or contact the organizing committee through PSMA via e-mail to power@psma.com .

www.psma.com

Gate Driver Portfolio Simplifies SiC Power Design for AI Data Centers and EVs

AHV85003/AHV85043 chipset joins the flagship AHV85311 integrated solution with complete family of noise-eliminating, self-powered SiC gate drivers



Allegro MicroSystems announced the strategic expansion of its Power-Thru™ isolated gate driver portfolio with the launch of the AHV85003/AHV85043 chipset. Joining the AHV85311 integrated solution, this expanded family creates a complete ecosystem for high-voltage silicon carbide (SiC) designs in AI data centers, electric vehicles (EVs), and clean energy systems. The solution simplifies the design challenge in power conversion by eliminating the need for external isolated bias supplies for gate drivers. This innovation delivers the industry's smallest solution footprint while reducing the bill of materials (BOM) to address the critical challenge of achieving maximum power density, especially in demanding 800V systems.

Allegro's Power-Thru isolated gate drivers integrate signal and power across a single isolation barrier. This breakthrough approach reduces common-mode capacitance in the system by up to 15x, addressing a major source of noise that impacts efficiency. They deliver up to a 20dB improvement in electromagnetic interference (EMI) performance, which boosts overall system efficiency and eliminates countless hours spent by designers resolving noise issues.

In addition to addressing the physics of noise, the expanded Power-Thru portfolio is engineered to resolve critical business challenges. To ensure supply chain resilience, both the new AHV85003/AHV85043 chipset and the existing AHV85311 integrated solution support a multi-source SiC strategy. With selectable gate-to-source voltages (Vgs) of 15V, 18V, and 20V, and adjustable regulated negative voltage, designers can easily swap between SiC FETs from different vendors without redesigning their boards.

Furthermore, the portfolio now offers two distinct implementation paths. The flagship AHV85311 integrated solution, which includes the isolation transformer, provides an all-in-one route for accelerating time-to-market. The versatile new AHV85003/AHV85043 chipset empowers designers to optimize for cost and layout by selecting their own external transformer tailored for their specific isolation needs.

"We are redefining what engineers should expect from a gate driver," said Vijay Mangtani, Vice President and GM of High Voltage Power Products at Allegro MicroSystems. "With Power-Thru, we solved the fundamental physics problem of noise in high-voltage systems. Now, by offering both a chipset and an integrated solution, we are giving our customers a complete toolkit. Whether they need the plug-and-play speed of an integrated solution or the granular control of a chipset, they get the same game-changing efficiency and the freedom to use the SiC FETs of their choice."

www.allegromicro.com

Multiphysics Simulation and Simulation Apps in Power Electronics

Why Single-Physics Models Just Don't Cut It Anymore

Electrification in transportation, energy, and other industries is driving new demands on power electronics, where performance and reliability depend on tightly coupled physical phenomena. Multiphysics-based digital twins are increasingly used to capture these interactions, enabling more accurate predictions and better-informed design choices. Simulation applications package these complex models into accessible, task-specific tools, allowing a wider range of stakeholders to contribute to the creation of high-performance, reliable systems.

By Bjorn Sjodin, SVP of Product Management, COMSOL

There is a global push for faster charging and smaller EV footprints, which in turn calls for power electronics to do more in less space. For engineers, these demands mean the old "siloed" way of working is dead. For instance, you cannot just optimize the electrical side of a system and then hand it off to the thermal team anymore. If the heat rises, the conductivity shifts; if the switching frequency climbs, you are suddenly dealing with vibration and acoustics issues you never saw in a static model.

These physics are not just "interacting"; they are actively fighting each other. Using simplified calculations or waiting for a late-stage physical prototype to find these issues slows down the process and is, frankly, a recipe for expensive field failures.

For example, in a modern inverter, physics phenomena do not occur in isolation but rather *cascade*. When semiconductors dump heat into busbars, cooling is not the only issue. Temperature changes electrical conductivity, which shifts switching behavior and alters magnetic properties. Meanwhile, thermal gradients introduce mechanical stress that slowly deforms solder joints and bond wires. These hidden interactions are often what kill a design in the field.

Two examples of hidden interactions to look out for include:

- The fatigue trap: A design may look electrically sound and thermally stable on paper, but if you ignore cyclic mechanical stress, thermomechanical fatigue will take out bond wires or solder layers long before the expected lifetime.
- The transient gap: Steady-state models capture best-case conditions, but real systems rarely operate there. A cooling strategy that looks acceptable in a static analysis can fail once transient switching losses and fluctuating airflow come into play.

At this point, "close enough" is no longer good enough. A unified multiphysics framework offers higher accuracy and enables teams to catch expensive surprises in software, before a single prototype reaches the test bench.

Benefits of Simulation Apps and Digital Twins

Multiphysics models can be complex to handle for those who do not work with simulations on a daily basis. One solution to making the integration of simulation easier is through the use of simulation apps, which are task-specific tools built on high-fidelity models. They have specialized user interfaces that expose only the parameters relevant to a given decision, such as geometry dimensions, material properties, or operating conditions (such as ambient temperature). The underlying physics remain consistent and controlled, and the user does not need to be an expert in the underlying simulation machinery or even have to open the full simulation environment.

Physics models can also be packaged into digital twins that use minimal sets of inputs and outputs. In practice, a digital twin may be implemented as a simulation app or through custom programs written using APIs, often integrated with other software services. A digital twin represents a virtual counterpart of a physical system, one that reflects geometry, materials, boundary conditions, and operating scenarios and can be revisited throughout development. Digital twin technology is still evolving, especially in power electronics. Today, digital twin concepts are most often discussed as a way to:

- Predict temperature distributions and identify hotspots under realistic load cycles
- Evaluate electrothermal and thermomechanical stress during power cycling
- Assess how material choices, packaging concepts, and cooling strategies interact

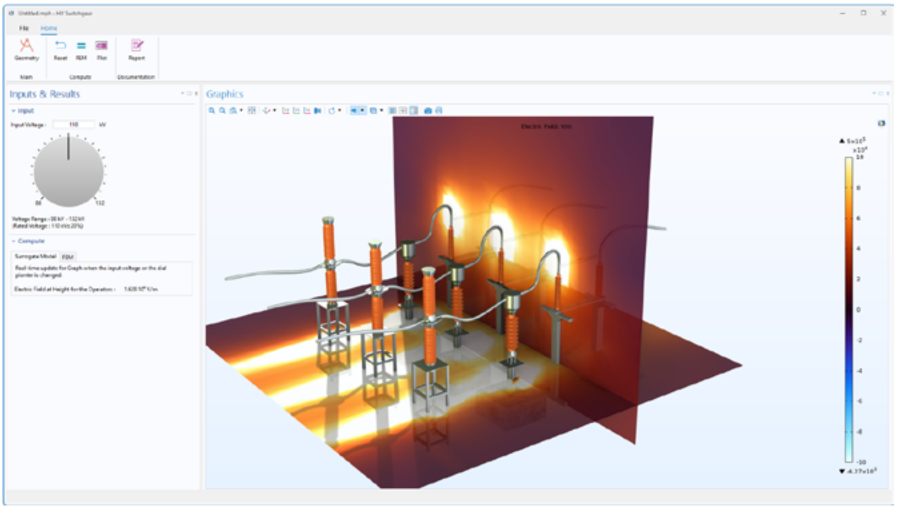


Figure 1: An example surrogate model for an HV switchgear. This app can be used to analyze how electric potential distribution affects input voltage.

- Support design tradeoffs involving efficiency, power density, and lifetime
- Improve continuity between design assumptions and real operating behavior

When rapid feedback matters more than full detail, reduced-order or surrogate models (Figure 1) can be used. Trained on simulation data, these models are based on machine learning techniques and can reproduce system behavior in a fraction of the time, making them well suited for interactive studies and early-stage exploration. More recently, GPU acceleration has been used to speed up both the training of surrogate models and the solution of full-scale simulation models.

In practice, the implementation of simulation apps and digital twins varies widely, but however they are used, they offer a feasible way to bring simulation into day-to-day engineering work. For instance, a common antipattern in R&D is the back and forth between production teams and modeling specialists for every design iteration. Each change requires another round of setup, simulation, and interpretation, turning advanced analysis into a workflow bottleneck. Simulation apps break that cycle and put physics-based insight into more hands: Design engineers can compare concepts early, and manufacturing teams can examine the influence of process parameters. System specialists can explore operating conditions using the same underlying assumptions. Even sales departments can make use of simulation apps. As one example, sales engineers used simulation apps to demonstrate the impact of design changes in real time in meetings with customers.

Multiphysics Modeling with COMSOL Multiphysics®

The COMSOL Multiphysics® software provides a unified environment for both multiphysics modeling and simulation app development through its Application Builder. Rather than stitching together separate tools, engineers can combine multiple physics interfaces directly within a single model. For power electronics, teams can combine:

- Electromagnetic modeling of currents, fields, and inductive and capacitive effects
- Thermal analysis covering Joule heating, electromagnetic losses, and radiation
- Fluid–solid–thermal dynamics for natural and forced convection cooling as well as conjugate heat transfer
- Structural mechanics for thermal expansion, stress, and fatigue
- Semiconductor device modeling for MOSFETs, IGBTs, diodes, and wide-band-gap materials

In power electronics, changes in one domain immediately influence the others, either locally or at some distance, such as for magnetic couplings. This reaction makes coupling for predicting how high-power, high-density designs behave outside the simulation environment.

The following case studies illustrate how companies are using multiphysics modeling and simulation apps to handle these interactions in practice. The examples are drawn from real industrial projects, but the company identities are omitted.

Case Study:
Electrothermal Optimization of EV Power Electronics

In EVs, inverters and DC link capacitors strongly influence efficiency, driving range, and reliability. A global automotive supplier used multiphysics simulation to redesign these components for next-generation electric drivetrains.

By coupling electromagnetic and thermal analyses, engineers identified local hotspots in DC link capacitors early in development (Figure 3). This insight made it possible to adjust geometry, materials, and cooling concepts before building hardware prototypes.

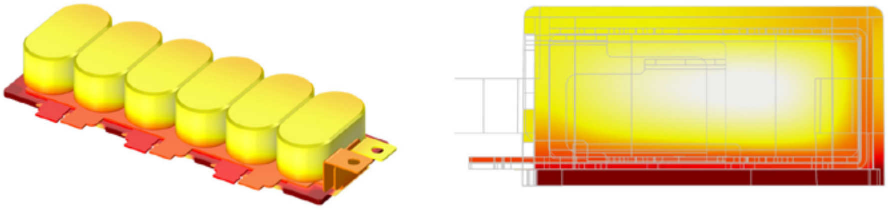


Figure 3: Left: the thermal effects inside of a DC link capacitor design. Right: a cutaway view of the capacitor model showing a hotspot. Image credit Bosch.

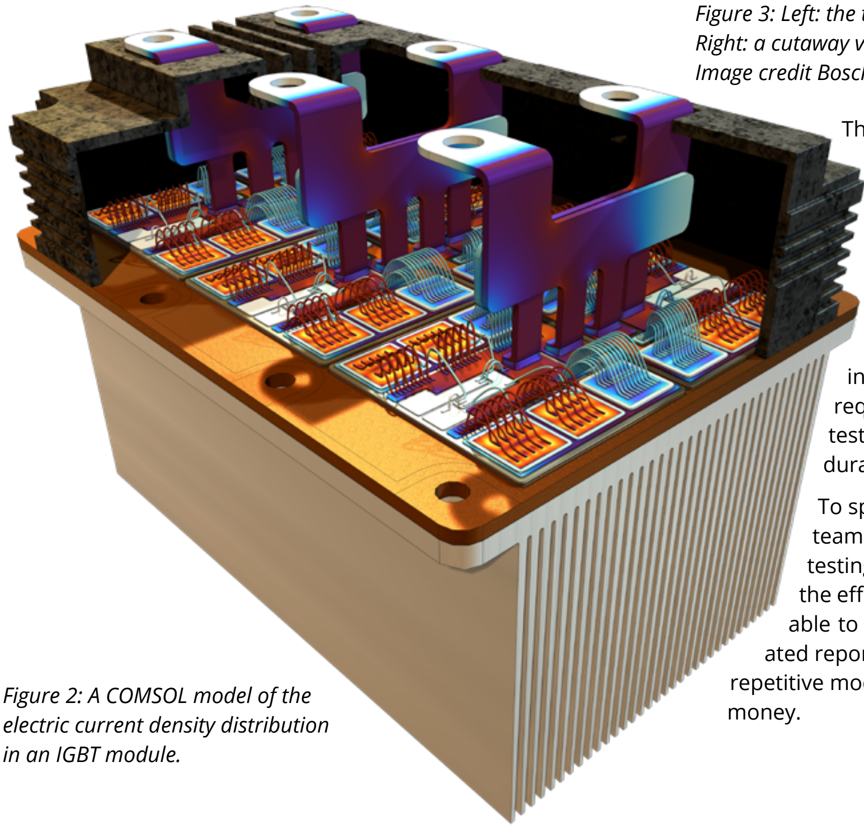


Figure 2: A COMSOL model of the electric current density distribution in an IGBT module.

The result was a new generation of optimized inverters with higher power density and extended vehicle range, offering one example of how multiphysics-based simulation supports system-level performance improvements.

Case Study: Simulation Apps Streamline EV Motor Development

Electric motor design involves a constant balancing act between electromagnetic and mechanical requirements. Using a multiphysics model alone to test and balance requirements such as torque and durability can quickly become time-consuming.

To speed up development, an automotive engineering team built a simulation app that could automate load testing of rotor laminations, making it easier to predict the effects of stress and benchmark designs. Users were able to quickly adjust parameters and even get a generated report that included strength ratings. The app reduced repetitive model setup and ultimately saved the team time and money.

Case Study: Custom Capacitor Design with Simulation Apps

Designing capacitors to meet application-specific requirements means balancing electric field stress, thermal behavior, and packaging constraints. Traditional workflows often require multiple rounds of simulation and refinement.

An engineering team at an electronic equipment manufacturer addressed this challenge by building simulation apps based on high-fidelity multiphysics models. The apps offered customized user interfaces where users could adjust parameters such as:

- Film geometry for a power film capacitor in order to determine the capacitance and resistance
- Film and winding characteristics for the metal film in a cylindrical capacitor in order to calculate power density
- Terminal properties of a single-tab film capacitor in order to calculate the effective series inductance (ESL)

With these apps, design teams and teams at manufacturing sites can test and compare ideas faster.

Case Study: Simulation Apps for Semiconductor Packaging Design

High-performance power electronics based on wide-band-gap semiconductors place strict demands on efficiency, thermal stability, and manufacturability. At a developer of silicon-carbide technologies, multiphysics simulation supported design decisions that involved electrical, thermal, and structural considerations. The engineers created multiple simulation apps that made it possible to simplify design analyses.

One app focused on the wires that connect semiconductor devices. With this app, the engineers could evaluate the fusing current and impedance of the wires in order to determine how many wires they needed. Another app made it possible to determine the temperature of high-performance power modules during operation.

These apps, and more, were used by the company's engineering team as well as supervisors and the marketing team. The different teams were able to assess real-world performance and better understand the products.

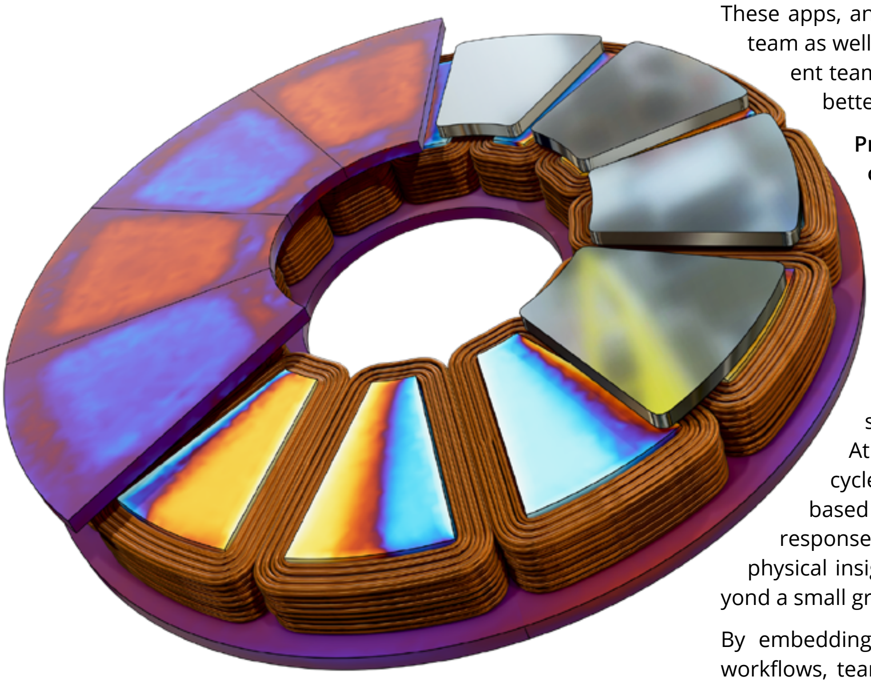


Figure 4: An example of a complex electric motor model that could be packaged into a simulation app.

Preparing for the Next Generation of Power Electronics

Power electronics sit at the center of electrification. Their performance and reliability depend on the interaction of electrical, thermal, mechanical, and fluid phenomena, interactions that single-physics approaches cannot fully capture.

Wide-band-gap semiconductors, higher switching frequencies, and tighter integration will only intensify multiphysics interactions in power electronics. At the same time, pressure to shorten development cycles and control cost continues to grow. Multiphysics-based simulation and simulation apps offer a scalable response. They support collaboration and preserve detailed physical insight while making advanced analysis accessible beyond a small group of specialists.

By embedding multiphysics directly into everyday engineering workflows, teams can move away from reactive troubleshooting and toward more predictive, model-driven development. Teams that integrate this development approach will be better positioned to deliver reliable, high-performance power electronics for the next generation of energy and mobility systems.

COMSOL Multiphysics is a registered trademark of COMSOL AB.

www.comsol.com

Effect of Optocoupler Parameter Variations on the Control Loop of a Power Supply

Isolated power supplies with secondary-side regulation need a feedback path to the primary side across the galvanic isolation. Very common is the use of a optocoupler in the feedback path. Which role do parameter variations of optocouplers play in this context?

By Eleazar Falco, Senior Application Engineer, Würth Elektronik

Among isolated power supplies, secondary-side regulation is commonly used when tight output voltage regulation and fast transient response are essential requirements. With this technique, the output voltage feedback signal needs to be transferred across the isolation barrier, from the output stage on the secondary side to the controller on the primary side, and optocouplers are commonly used for the task. However, the role of the optocoupler in the system is not limited to this, since it is also part of the compensator circuit and parameters like its CTR (current-transfer-ratio) and output parasitic capacitance will modify the magnitude and phase of the feedback signal. Thus, they appear in the compensator transfer function, helping to shape its frequency response and in turn, contributing to set the stability margins of the converter's control loop.

If the parameters were constant, the design and worst-case analysis would be considerably eased, but this is not the case. The optocoupler CTR has a wide production tolerance, to which further variations over DC-bias, temperature and lifetime of the device must be accounted for (Ref[1], Ref[2]). In addition to this, the optocoupler parasitic capacitance is also dependent on the same parameters as well as on the device's CTR itself. Thus, for a reliable and functionally robust design, an assessment of the impact that such parameter variations have on the stability margins of the converter is required, considering all expected operating conditions. For this, a practical experimental approach can be followed, as presented in this article.

The optocoupler in the compensator circuit

A typical optocoupler-based type-2 compensator circuit using a voltage reference (TL431) as error amplifier is shown in Figure 1. The circuit receives the converter output voltage (V_{out}) as the input and provides a voltage level at its output (V_{CO}), which is fed to the current-mode PWM generator block (not shown). Note how V_{CO} corresponds to the collector-emitter voltage of the optocoupler phototransistor. Such a compensator circuit is widely used to stabilize the feedback loop of a current-mode flyback converter operating in continuous-conduction-mode (CCM).

The transfer function of this compensator circuit in the Laplace s-domain is as below (Ref[4]):

$$C(s) = \frac{V_{co}(s)}{V_{out}(s)} = -G_m \cdot \frac{\left(1+\frac{\omega_z}{s}\right)}{\left(1+\frac{s}{\omega_p}\right)} = -\left(\frac{R_c \cdot CTR}{R_{LED}} \cdot \frac{R_2}{R_1}\right) \cdot \frac{\left(1+\frac{1}{s \cdot R_2 \cdot C_1}\right)}{\left(1+s \cdot R_c \cdot (C_{col}+C_{opto})\right)} \quad (E.1)$$

Observe how the CTR affects the term G_m (a.k.a. midband Gain), while the phototransistor parasitic capacitance (C_{opto}) affects the pole frequency (ω_P).

Selecting a WL-OCPT 817 optocoupler from the bin 'B' means that the DC-CTR tolerance out-of-production will be between 1.3 and 2.6 (Ref[3]), measured with a DC-bias of V_{CE} = 5 V and I_{LED} = 5 mA. But in the converter operating in closed loop, the compensator output voltage and in turn, the optocoupler DC-bias point is set by operating conditions like input voltage and output current. Thus, the new CTR range for the DC-bias point representing worst-case condition needs to be obtained.

The example design used in this article is a flyback converter with the following basic specification: V_{in} = 36 to 57 V, V_{out} = 12 V, I_{out} = 3 A and F_{sw} = 300 kHz. The transformer used is the WE-POEH 7491195112 from Würth Elektronik and the controller IC the NCP12700 from Onsemi. The equivalent output capacitance is 100 µF with ESR of just a few hundreds of µΩ (shifting the ESR zero to the MHz range with no influence on the plant response (Ref[4])).

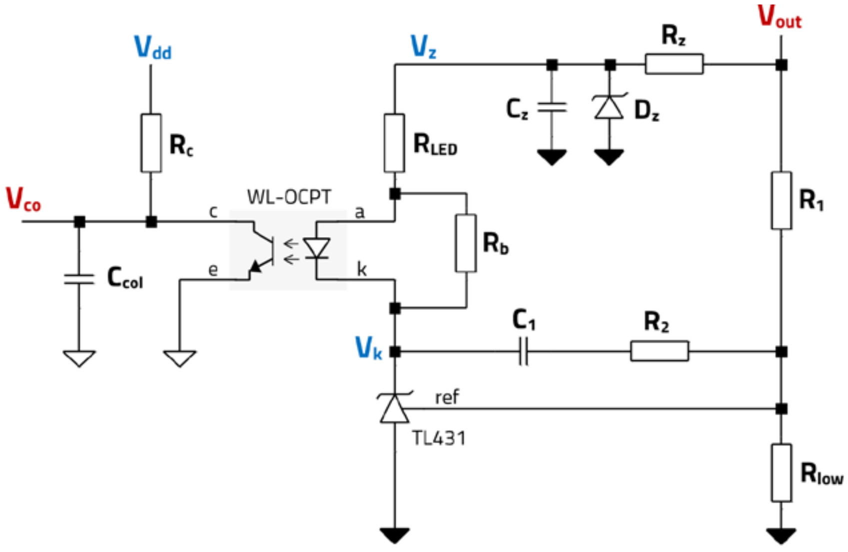


Figure 1: Optocoupler-based type-2 compensator with TL431

The compensator is designed for the worst-case condition of the control-to-output transfer function, corresponding to minimum input voltage (36 V) and full-load current (3 A) (i.e. where the right-half-plane-zero is at the lowest frequency). At this operating point, the compensator (and optocoupler) output voltage is V_{CO} = 2.7 V (Ref[4]). With V_{dd} = 5 V and R_C = 5 kΩ fixed by the NCP12700, then a phototransistor current of I_C = 0.46 mA results.

Measuring optocoupler CTR and parasitic capacitance (C_{opto})

The CTR at this DC-bias condition (V_{CO} = 2.7 V and I_C = 0.46 mA) can be obtained in different ways. One of them is by using the CTR vs. I_{LED} curve provided in the WL-OCPT 817 series datasheet (Ref[3]), while another approach can be to run a SPICE simulation with the freely provided WL-OCPT SPICE models.

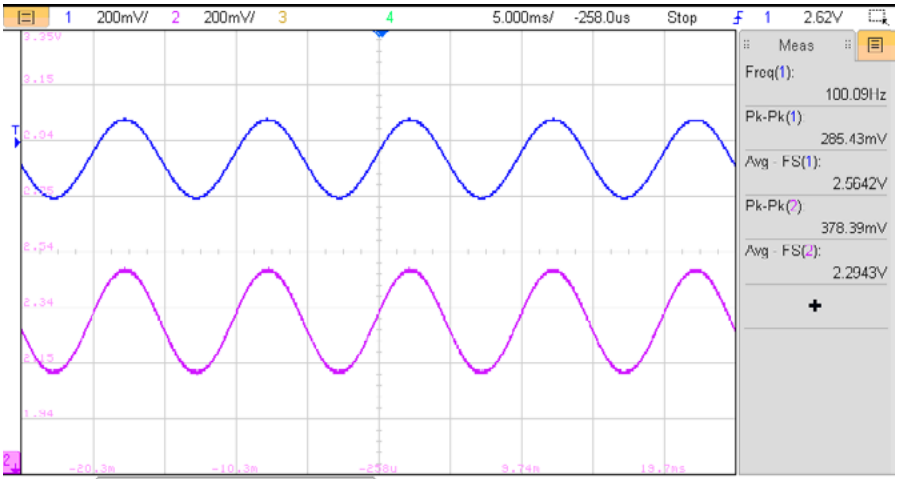


Figure 2: Optocoupler DC and AC CTR measurement (I_{LED} – blue, I_C – violet)

However, there is no more accurate approach than to measure it directly. For this, a WL-OCPT 817 sample device from bin 'B' with a CTR close to the average of the bin's range at the reference test DC-bias conditions should be used (i.e. ideally CTR_{AV} = 1.95 at V_{CE} = 5 V, I_{LED} = 5 mA). In this case, the reference device used had a DC-CTR of 2.08, close to the average of the binning, and its LED and phototransistor currents at V_{CE} = 2.7 V are shown in Figure 2, measured as voltages across 5 kΩ resistors (I_{LED} (blue) and I_C (violet)). The DC currents are I_C = 0.46 mA (i.e. 2.29 V / 5 kΩ) and I_{LED} = 0.512 mA (i.e. 2.56 V / 5 kΩ). The ratio of the DC voltages corresponds to the DC-CTR, in this case equal to 0.9 (i.e. 2.29 V/2.56 V).

Observe how a small amplitude, low frequency AC sinusoidal current is also superimposed to the DC current across the LED. Here, the ratio of the measured amplitudes corresponds to the small-signal or AC-CTR, which at this operating point is 1.3 (i.e. 378 mV/285 mV).

For the DC-biasing of the optocoupler and TL431 in the compensator circuit, the DC-CTR is used for relevant component calculations, whereas for control loop stability and dynamic behavior of the compensator circuit, where small amplitude AC signals are considered, the small-signal AC-CTR should be used. Note that there are some cases where both DC and AC CTR values are close enough, so that the DC-CTR can then be used as an approximation (e.g. as in Ref[4]). But this is not always the case.

With the DC and AC CTR values already known, C_{opto} needs to be measured before advancing to the compensator design. The measured frequency response of the bin 'B' reference sample used, biased at V_{CE} = 2.7 V and I_C = 0.46 mA, with R_C = 5 kΩ as in the compensator circuit, is shown in Figure 3.

The corner frequency is around 18 kHz, and with this, the nominal C_{opto} can be calculated:

$$C_{opto} = \frac{1}{2 \cdot \pi \cdot R_c \cdot f_{p\_opto}} \approx 1.77\ \text{nF}$$

Observe how the Magnitude curve in the lower frequency range below 1 kHz is mostly 'flat' at a value of 2.325 dB, which corresponds to the AC-CTR of 1.3.

Compensator Design and Stability analysis

The compensator is designed to achieve an open-loop cross-over frequency of 2 kHz and a phase margin of 60°. At 2 kHz, the plant transfer function has a magnitude of 1.32 dB and a phase of -71° (Figure 4). Thus, the compensator response needs to have a magnitude of -1.32 dB and a phase of 131° at 2 kHz. For this, the following compensator component values are selected: R_2 = 5.6 kΩ, C_1 = 33 nF and C_{COL} = 4.7 nF. The procedure followed for this calculation and for the rest of the components of the compensator circuit of Figure 1 goes beyond the scope of this article, but it is covered in detail in Ref[4].

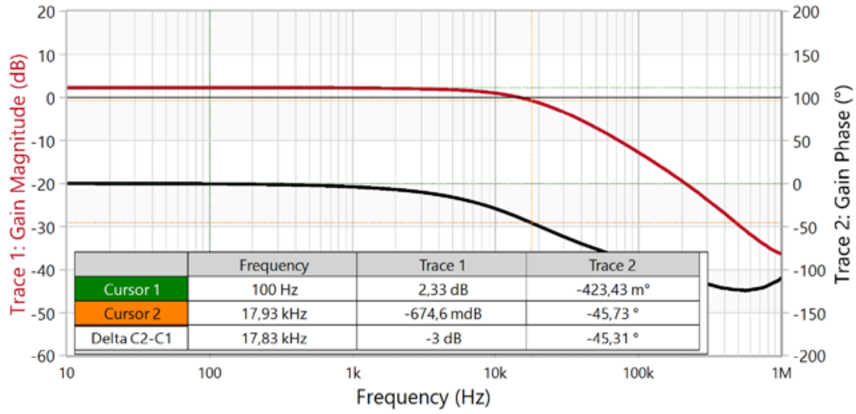


Figure 3: Frequency response of WL-OCPT 817 bin B sample

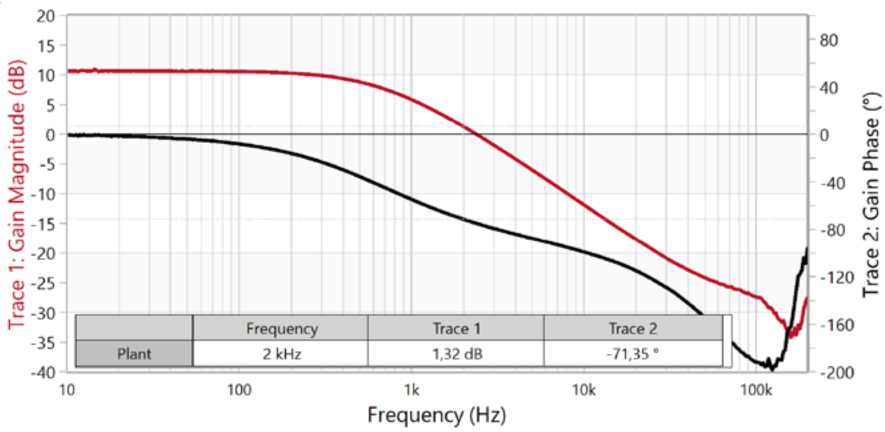


Figure 4: Plant transfer function with measured magnitude and phase at 2 kHz

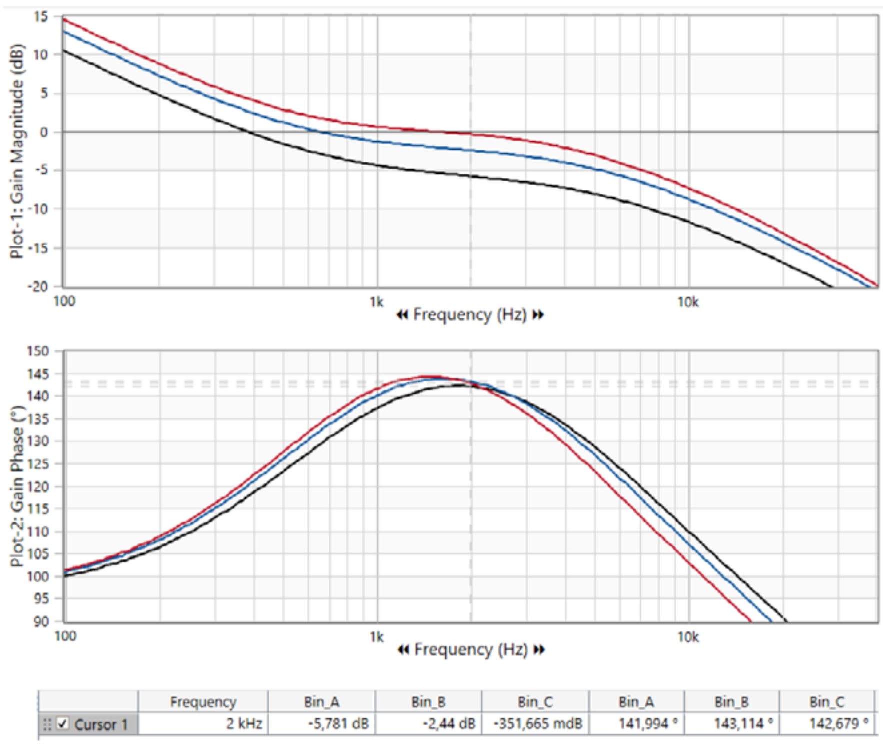


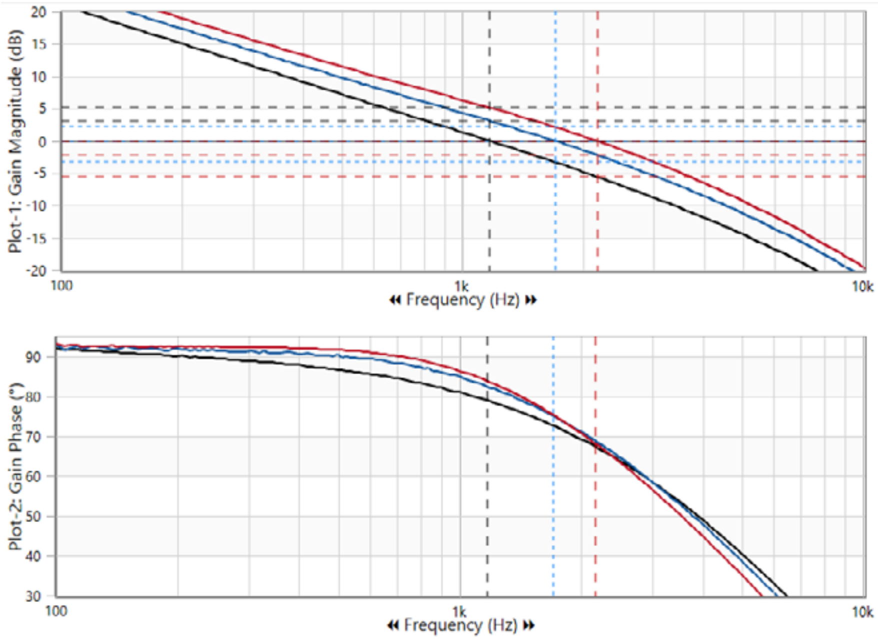
*Figure 5: Measured frequency response of compensator with CTR variations of WL-OCPT 817 bin B (min (red), nom (blue), max (**black**))*

As mentioned before, the bin 'B' has a CTR production tolerance of around ±30%. With a nominal DC-CTR value of 0.9 for the DC-bias conditions of this design, this results in a CTR range between 0.6 and 1.2. In order to experimentally assess the impact of this production tolerance on the converter stability margins, a WL-OCPT 817 device from bin 'A' having a DC-CTR of 0.61 and a sample from bin 'C' with a DC-CTR of 1.22 (both measured at V_{CE} = 2.7 V with R_C = 5 kΩ as in this design) can be used, as they are slightly above and below the estimated CTR limits of the bin 'B'. Their measured AC-CTR values are 0.84 and 1.83 for the bin 'A' and bin 'C' sample, respectively.

Note that the CTR and C_{opto} are directly related: a device with a higher CTR will suffer from a higher C_{opto} for the same DC-bias condition, and vice versa. The frequency response for the bin 'A' and bin 'C' devices is also measured, obtaining corner frequencies of 24.4 kHz and 12.5 kHz, respectively. These, in turn, correspond to C_{opto} values of 1.3 nF for the bin 'A' device and 2.6 nF for the bin 'C' device. This capacitance variation will shift the compensator pole to lower and higher frequencies, respectively, compared to the nominal case of the bin 'B' sample used for the design. Observe how the bin 'A' sample represents the minimum expected values of CTR and C_{opto} of the bin 'B', while the bin 'C' sample represents the maximum ones.

Figure 5 shows the measured Bode plot of the compensator transfer function for these three samples: bin 'A' (red), bin 'B' (blue) and bin 'C' (black). A change in the midband gain (see around 2 kHz) is clearly observed while the variations in the pole frequency are less obvious due to the wide frequency range covered on the X-axis. Finally, Figure 6 shows the open-loop frequency response, where a crossover frequency variation between 1.1 and 2.2 kHz can be observed. In this example, the phase margin, which determines stability, remains high between 68° and 79°, despite a rather wide variation of the optocoupler parameters.

In addition to this, the impact of operating temperature variations over the expected range must also be studied. Here, a thermal chamber will help to perform this evaluation experimentally with the previous samples. Another factor to consider is the optocoupler's LED degradation with operating



	Frequency	OL_BinA	OL_BinB	OL_BinC	OL_BinA	OL_BinB	OL_BinC
Bin A	1,169 kHz	0 dB	3,115 dB	5,151 dB	79,146 °	82,584 °	83,887 °
Bin B	1,702 kHz	-3,319 dB	0 dB	2,146 dB	72,805 °	75,265 °	75,461 °
Bin C	2,169 kHz	-5,556 dB	-2,179 dB	0 dB	67,482 °	68,899 °	68,282 °

*Figure 6: Measured frequency response of open-loop transfer function with CTR variations of WL-OCPT 817 bin B (min (red), nom (blue), max (**black**))*

time, and Ref[2] provides guidance for this. However, when operating at low LED currents and a not too high ambient temperature as in this design, the influence of the LED degradation will be negligible. For reference, the DC-DC converter prototype used for the measurements is shown in Figure 7.

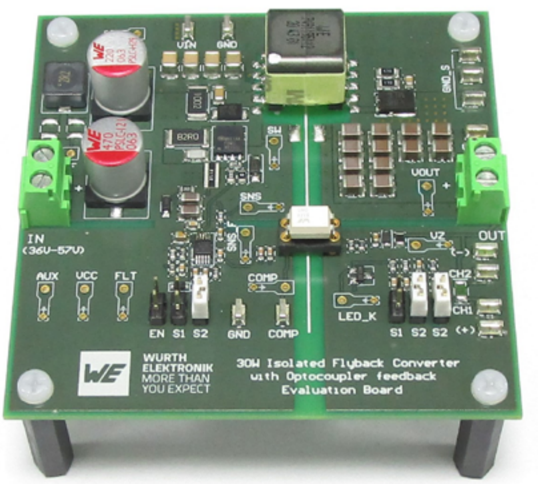


Figure 7: 30W Flyback converter prototype board

Conclusion

Evaluating the impact of optocoupler parameter variations on the stability margin of a power supply's feedback loop is key to ensure reliable operation over the converter's operating life. This article showed an example approach to do this based on real measurements, instead of simulations or calculations.

This is partly made possible by the tight CTR binning classification that Würth Elektronik provides for its WL-OCPT™ optocouplers.

References

[1] Application Note ANO007 – Understanding Phototransistor Optocouplers, Würth Elektronik: www.we-online.com/ANO007

[2] Application Note ANO006 – Lifetime of Optocouplers, Würth Elektronik: www.we-online.com/ANO006

[3] Optocoupler OCPT 817 Series, Würth Elektronik Datasheet: https://www.we-online.com/en/components/products/WL-OCPT_PACKAGE_DIP-4

[4] Application Note ANP113 – Feedback loop compensation of a current-mode flyback converter with optocoupler, Würth Elektronik: www.we-online.com/ANP113

www.we-online.com

On-Chip Redundancy and the Myth of Independence

Redundancy is a numbers problem; Independence is an architectural one!

Redundancy is often treated as a numbers problem: add more blocks, duplicate critical functions, and safety improves. In battery management ICs, this has led to designs that advertise multiple ADCs and parallel signal paths as evidence of robustness.

By Ahmad Ashrafzadeh, CEO/CTO, Nova Semiconductor

At Nova, we recognized early that dedicated ADCs per cell are essential for truly independent and reliable measurements, and our work has helped shape industry thinking around this requirement. This trend underscores why understanding measurement independence, and not just the number of ADCs, is critical for modern BMS architectures.

But redundancy alone does not guarantee safety. What matters is independence.

When redundant functions share critical dependencies, such as voltage references, bias networks, multiplexers, clocks, or assumptions embedded in firmware, they form correlated failure domains. In those cases, a fault does not reveal itself through disagreement; it propagates identically through every "redundant" measurement. The system appears healthy while being uniformly wrong.

This distinction is especially important in BMS designs, where measurement accuracy underpins impedance estimation, balancing, fault detection, and protection decisions. If a common-cause failure affects measurements in the same way, whether through shared analog infrastructure or through die-level effects that impact multiple on-chip blocks, redundancy becomes an illusion rather than a safeguard.

This article examines two frequently overlooked aspects of this problem: shared dependencies within groups of on-chip ADCs, and the limits of redundancy implemented entirely within a single IC. By dissecting why these couplings matter, and why they persist, we can better understand what true measurement independence requires in modern BMS architectures.

Why Shared ADC References Undermine Measurement Independence

A common misconception in BMS IC design is that multiple ADCs automatically provide independent measurements. In reality, when a group of ADCs shares a single voltage reference, their readings are tightly coupled, and any error in the reference propagates identically across all measurements.

Consider a set of 16 ADCs within a single IC. Each ADC samples a different cell voltage, but all draw from the same reference. If the reference drifts due to temperature, aging, or electrical stress, all 16 measurements shift together. From a redundancy standpoint, the ADCs continue to "agree" with each other, giving the false appearance of accurate and consistent data. In practice, the system cannot distinguish between a true measurement and a correlated error caused by the shared reference.

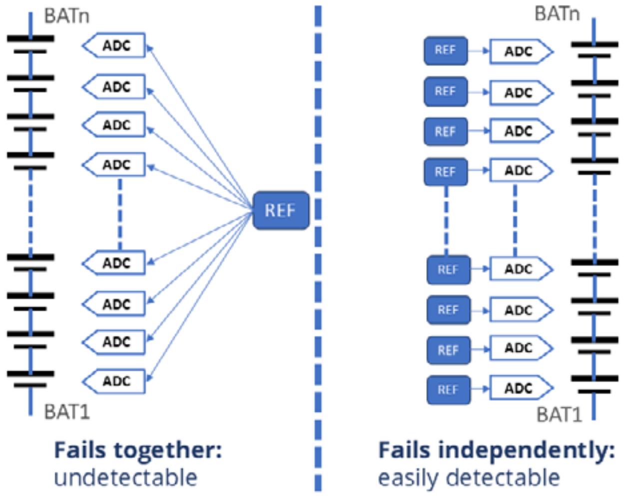


Figure 1: Shared references create correlated errors; independent references allow faults to be detected.

This correlated error is particularly problematic for BMS functions that depend on precise measurements, such as:

- **Impedance estimation:** small voltage differences define the calculated cell impedance. A reference shift introduces a uniform offset across all cells, skewing calculations.
- **Balancing decisions:** automatic balancing relies on relative voltage differences. A uniform error can cause unnecessary balancing or leave imbalances undetected.
- **Fault detection and protection:** threshold-based alerts may fail to trigger if all cell readings shift equally.

Importantly, this problem is structural, not an occasional glitch. It exists in every IC where multiple ADCs share a reference, independent of ADC resolution or speed. High-resolution ADCs amplify the visibility of the error: the measurements remain internally consistent, but systematically wrong.

By clearly separating ADC measurement independence from ADC count, we can understand why simply "adding more ADCs" is insufficient. True measurement independence requires either dedicated references for each ADC or an architecture that can digitally decouple ADC readings from a single reference.

Redundant On-Chip ADCs and the Limits of True Redundancy

Adding a second ADC on the same die is often presented as a redundancy measure. At first glance, two measurement channels appear to offer protection: if one fails, the other can detect disagreement or take over. However, most real-world failures in ICs are broadly coupled across the chip, meaning that both ADCs are affected simultaneously.

Vincotech

TAMING THE FUTURE

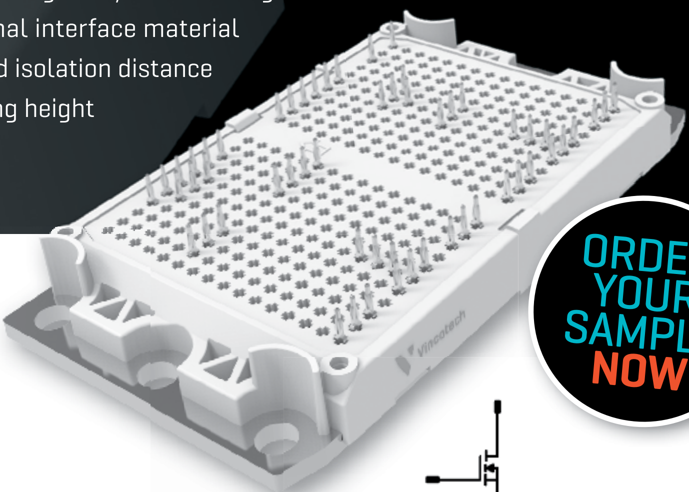
Pushing the leading edge of PV & ESS further

Vincotech's latest generation of base-plated housings enables PV & ESS system designers to push the leading edge of the renewable energy even further. The new *flow* E3BP supports development of 350 kW and beyond thanks to the optimally shaped baseplate which ensures superior thermal contact. This leads to excellent thermal performance and maximized power density.

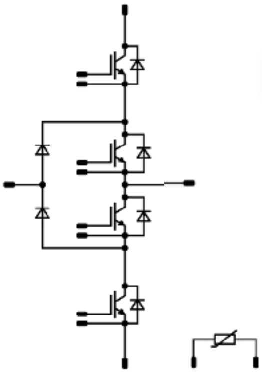
The housing material is specifically chosen to meet the voltage requirements of the next generation 2000 V systems. Depending on the application requirements, configurations are available with either Si or SiC devices.

flow E3BP features

- Convex baseplate with special surface treatment for superior thermal contact
- CTI600 housing material for higher systems voltages
- Optional pre-applied thermal interface material
- Isolation walls for increased isolation distance
- 12 mm and 15 mm mounting height
- Solder or Press-fit pins

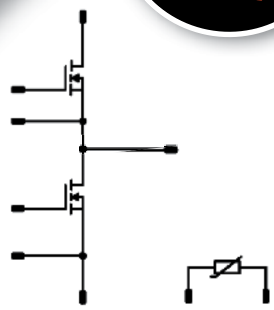


ORDER YOUR SAMPLE NOW



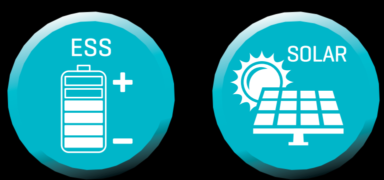
/ **350 kW Utility String PV**
30-EP12NIA600H701-PM00F87T

/ **250 kW Utility ESS/PCS**
30-EP12NIA400H7-PM40F07T



/ **Latest 2.3 kV SiC MOSFET technology**
30-EP232PB004ME01-PR09F07T

* Several other modules are in development, in addition to those shown



Vincotech.com/flowE3BP

EMPOWERING **YOUR IDEAS**

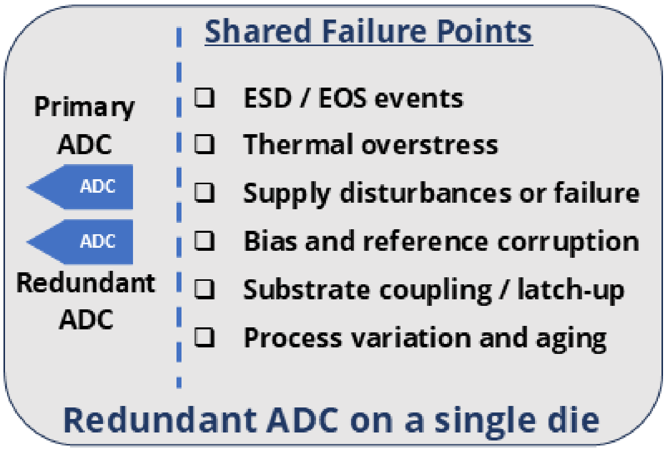


Figure 2: Redundant ADCs on one die share failure mechanisms and do not provide true independence.

Common-cause failures that impact multiple on-chip blocks include:

- **Thermal overstress:** excessive heat affects the entire silicon die, including both ADCs
- **Overvoltage or ESD events:** stress propagates through shared substrate and power networks
- **Process variations and aging:** shifts in matching or bias circuits affect all analog blocks
- **Latch-up or substrate current events:** impact multiple analog and digital domains at once

When a failure affects both the primary and the redundant ADC, there is no disagreement; both channels continue to report similar values, potentially masking faults. The system assumes redundancy exists, but the actual failure domain has not been separated, leaving the measurement and protection functions vulnerable.

This limitation demonstrates that physical redundancy on a single IC does not guarantee measurement independence. Even if each ADC uses a separate reference, many critical dependencies remain shared. A comprehensive approach to measurement independence requires addressing these cross-channel couplings at the architectural level — something that cannot be solved simply by duplicating blocks on the same die.

Digitally Assisted Analog: Solving the Scaling Challenge

One of the key obstacles to achieving true measurement independence in BMS ICs is practical scaling. In conventional analog designs, adding more ADCs quickly becomes expensive: each additional ADC consumes area, increases power, requires extensive testing and trimming, and demands careful calibration. Attempting to duplicate references along with ADCs makes the problem even worse; there simply isn't enough die area, and design complexity grows disproportionately. As a result, engineers are forced into compromises, sharing references or minimizing the number of ADCs, which introduces correlated measurement errors and undermines redundancy.

Digitally Assisted Analog (DAA) addresses this challenge by shrinking the analog footprint of each ADC. Calibration, error correction, and signal conditioning are moved into the digital domain, making it feasible to replicate ADCs without the traditional area or power penalty. With smaller ADCs, it also becomes practical to implement dedicated references for each channel, solving the problem of correlated measurement error within each ADC group (Problem 1). Of course, this approach only works when all components are highly accurate. Multiplying ADCs and references with large error margins would exacerbate the problem rather than solve it.

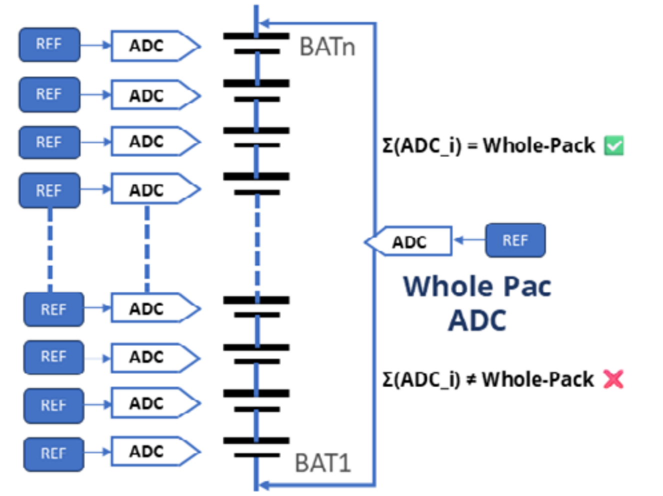


Figure 3: A quick and robust way to detect errors: a mismatch between full-pack voltage and the sum of cell ADCs indicates a measurement fault.

DAA also partially addresses Problem 2. By measuring the full pack voltage with an independent reference and comparing it against the sum of individual cell voltages, designers can catch some faults that would otherwise affect multiple ADCs on the same die.

While this does not replace true redundancy, which would require physically separate ICs, it provides a simple, practical method to introduce a meaningful level of redundancy without dramatically increasing system complexity.

The result is a scalable, architecturally sound approach where each cell voltage is measured independently, correlated errors are minimized, and the measurement system is robust enough for high-channel-count packs.

Conclusion

Redundancy in battery management ICs is not a matter of simply adding more ADCs or duplicating measurement paths. True safety and measurement integrity depend on independence: isolating failure domains so that a fault in one path does not propagate to others.

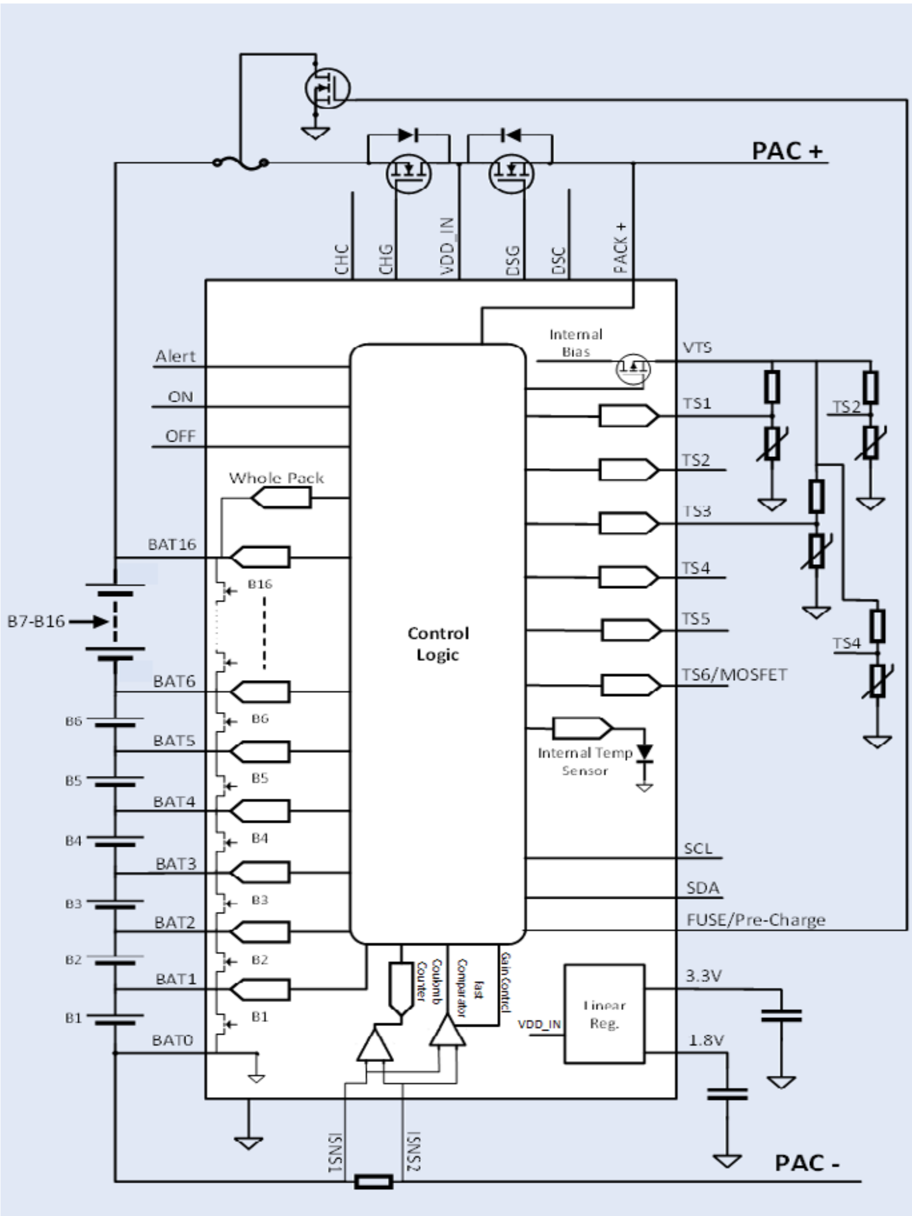


Figure 4: Detailed NB1600 architecture: scalable per-cell ADCs, full-pack measurement, and digitally assisted analog enable precise, reliable battery management. Every ADC channel uses a dedicated reference to ensure true independence.

Two key challenges limit conventional analog designs: shared references within ADC groups introduce correlated measurement errors, and redundant ADCs on a single die cannot fully protect against chip-level faults. Adding components alone does not guarantee reliable measurements or meaningful redundancy.

The NB1600 demonstrates how these challenges can be addressed in practice. Using Digitally Assisted Analog, every cell ADC, as well as the full-pack ADC, has its own independent reference, minimizing correlated errors and enabling meaningful redundancy without excessive area or power. As we at Nova have emphasized, dedicated ADCs per cell are essential for truly independent and reliable measurements. This design principle that has helped shape industry thinking. While true redundancy still requires physically separate ICs, this approach provides a practical, scalable path to high-accuracy, high-channel-count BMS designs.

Ultimately, evaluating redundancy requires asking the right questions: Are your measurement paths truly independent? Are your failure domains separated? Only by addressing these questions can designers ensure that their BMS provides both accurate cell-level data and meaningful protection.

www.novasemi.com

0.2% high-accuracy open-loop Hall Current Sensor with ASIL D functional safety

Hall current sensors have significantly improved their detection accuracy through error compensation while maintaining their original cost advantage. This article focuses on comparing the performance of Innosense's Dhips$^+$ Hall current sensor before and after error compensation, elaborating on the detailed architecture of functional safety, and introducing its product series.

By Wang Bowen, Global Product Director of Innosense

With the rapid development of power electronics technology today, as a core sensing component, the accuracy, reliability, and cost control of current sensors directly affect the performance and market competitiveness of end products. Although traditional Hall current sensors are widely used in industrial control, new energy vehicles, power systems and other fields due to their non-contact measurement, cost advantages and other characteristics, but the pain point of insufficient accuracy has always restricted the breakthrough in high-end application scenarios. The new generation of 0.2% high-accuracy Hall current sensor Dhips$^+$ series product launched by Innosense breaks the industry curse of "high accuracy must mean high cost" through core algorithm innovation, magnetic core technology optimization and full-link performance improvement, reshaping the value curve of Hall current sensors, and brings a revolutionary technical solution to the power electronics industry.

Industry Status: Value Dilemma and Technical Bottlenecks of Hall Current Sensors

The development of current detection technology has always centered around four core dimensions: "accuracy, cost, volume, and reliability". As one of the most widely used technical routes, Hall current sensors have long faced the challenge of balancing performance and cost. Open-loop Hall current sensors realize current measurement by detecting the magnetic field generated by current-carrying conductors based on the Hall effect principle. Their non-contact measurement method avoids interference with the main circuit, and their small size and fast response characteristics make them occupy an important position in various electronic devices. The mature supply chain system also gives them a significant cost advantage. However, the accuracy of traditional open-loop Hall current sensors has always been unsatisfactory, especially in small current detection scenarios. Errors caused by hysteresis effect, temperature drift, external interference and other factors make it difficult to meet the application requirements of high-end industrial control, new energy vehicle battery management systems (BMS) and other fields that have strict requirements for detection accuracy.

A comparison of the performance of current sensors based on different principles further highlights the industry's choice dilemma. Although closed-loop Hall current sensors have high accuracy, the complex feedback circuit design leads to a significant increase in cost, as well as large volume and high power consumption in large current scenarios; the shunt resistor scheme has a relatively low cost, but there is a prominent problem of heat generation in contact measurement, which brings potential safety hazards to the customer's system; fluxgate sensors have excellent accuracy, but they also face the shortcomings of high cost and poor anti-interference ability. In core application fields such as new energy vehicles, photovoltaic inverters, and accuracy industrial control, the market is urgently in need of a current sensor solution that can balance high accuracy, low cost, small size and high reliability. This demand has become the core driving force for promoting the technological innovation of Hall current sensors. Based on the above market demand for current sensors, Innosense has launched the high-accuracy Dhips$^+$ series current sensors, which originate from the in-depth deconstruction of the Hall detection principle and full-chain technological innovation. Through multi-dimensional technological breakthroughs such as hysteresis compensation algorithm, temperature stress compensation technology, and optimized magnetic core design, it has achieved a leapfrog improvement in accuracy performance while retaining the core advantages of traditional open-loop Hall sensors.

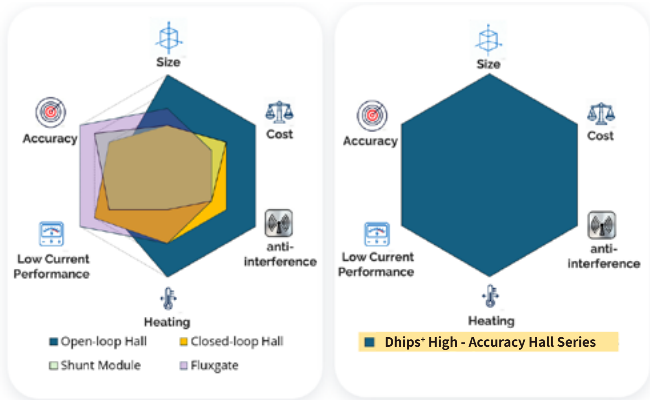


Figure 1: Innosense Dhips$^+$ & Other Principles Comparison

Technological Breakthrough: Core Innovation Path of High-Accuracy Hall Sensors

Multi-Dimensional Error Compensation Algorithm

The error compensation algorithm is the core support for the Dhips$^+$ series to achieve 0.2% high accuracy. Innosense has built a full-scenario algorithm system covering hysteresis compensation, temperature stress compensation, and dynamic compensation. The hysteresis effect is a key factor affecting the accuracy of Hall sensors. The hysteresis loops existing in different magnetic core materials during the magnetic field change process will lead to detection errors, which are more obvious in the small current range. The Dhips$^+$ series simulates the hysteresis characteristics of different magnetic core materials and structures, tests to obtain accurate hysteresis curves, refers to classic models such as Jiles-Atherton, and constructs static and dynamic hysteresis compensation models combined with actual application scenarios. Through a large number of experimental verifications and detailed optimizations, it achieves accurate cancellation of hysteresis errors. The offset error data before and after compensation shows that the error value before compensation is generally between 1~2A, and

DualPack3 Power Density, Simplified for You

Cost-Efficient Performance in Industry-Standard Packaging

The new DualPack3 modules with IGBT7 technology deliver power density, cost efficiency and robust performance in a compact, proven package. Available in 300–900A ratings at 1200V and 1700V, DualPack3 is built for today's demanding applications.

Key Features

- High power density in a smaller footprint
- Up to 20% reduced losses vs. IGBT4
- Compact 152 × 62 × 20 mm package size
- Higher current output without paralleling modules
- Simplified gate driving with precise dV/dt control
- Reliable operation up to 175°C overload temperature
- Supply chain security with multi-supplier support

Discover how DualPack3 can power your next design.

MICROCHIP

microchip.com/DualPack3

after compensation, the error is controlled within ±100mA, and in some working conditions, the error is even lower than ±20mA, with a significant compensation effect.

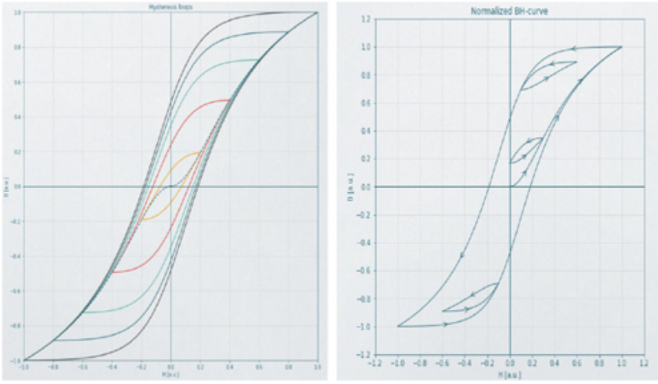


Figure 2: Hysteresis Loop Under Magnetic Field Interference

Temperature Stress Compensation Algorithm

The application of the temperature stress compensation algorithm solves the problem of accuracy drift in extreme environments. The output characteristics of Hall elements are significantly affected by temperature. The accuracy error of traditional sensors will increase sharply in the wide temperature range of -40°C to 125°C, while the Dhips^{+} series achieves stable control of accuracy in the full temperature range through the coupled temperature stress compensation algorithm. Test data shows that in the normal temperature environment of 25°C, the error of the Dhips^{+} series is controlled within ±0.2% in the full range of -1500A to 1500A; in the wide temperature range of -40°C to 125°C, the error can still be maintained within ±0.5%, meeting the application requirements of extreme environments.

Dynamic Offline Compensation Algorithm

In addition, the 100% offline dynamic compensation and segmented calibration functions further improve the consistency of the product. By performing offline dynamic calibration on each product, it automatically corrects individual differences to ensure the accuracy consistency of mass production; the segmented calibration function divides the measurement range into three segments for precise calibration, especially improving the resolution in the small current range, so that the Dhips^{+} series can still maintain excellent performance in small current scenarios. This is of great significance for battery current detection in new energy vehicle sentinel mode, micro-current monitoring in industrial control systems and other scenarios.

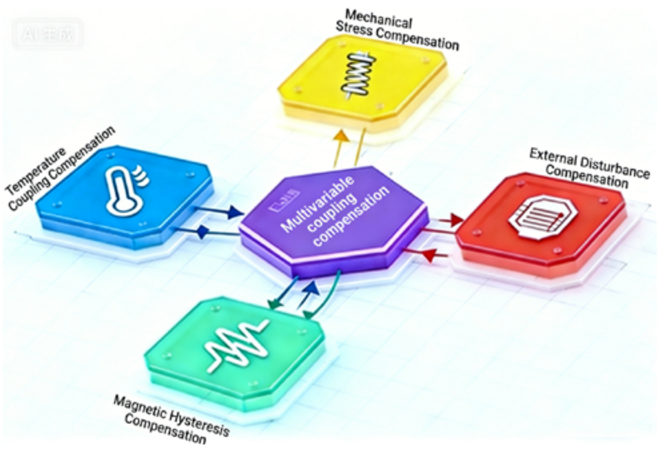


Figure 3: Innosense Dhips^{+} Product Compensation Algorithm

Product Performance: Redefining the Standard of High-Accuracy Hall Sensors

The performance of the Dhips^{+} series high-accuracy Hall current sensors has been fully verified through comprehensive test data and has reached the industry-leading level in key indicators such as accuracy, temperature adaptability, and consistency.

Accuracy Performance: Full-Range High-Accuracy Coverage

The core advantage of the Dhips^{+} series lies in its high-accuracy performance within the full range. This consistent high-accuracy performance across the full range breaks the problem of reduced accuracy of traditional sensors at small current or large current extreme points and meets the requirements of wide-range applications. The breakthrough in small current accuracy is particularly noteworthy. The accuracy of traditional open-loop Hall sensors often drops significantly in the small current range, while the Dhips^{+} series can still maintain excellent accuracy in small current scenarios through algorithm optimization and hardware improvement. This is of great value for small current detection of battery charging and discharging in new energy vehicle BMS and energy storage systems and can significantly improve the control accuracy and energy efficiency performance of end products.

Figure 4: Offset Error Before and After Hysteresis Compensation

Environmental Adaptability:
Stable Operation in Wide Temperature Range

In extreme temperature environment tests, the Dhips^{+} series showed excellent stability. In the low-temperature environment of -40°C, the output linearity of the sensor remains good, and the error does not drift significantly; in the high-temperature environment of 125°C, the performance of the Hall element is stable, and the accuracy error is still controlled within ±0.5% through the action of the temperature compensation algorithm. This wide temperature range adaptability enables the Dhips^{+} series products to be applied to harsh application scenarios such as northern frigid regions, new energy vehicles, and super-fast charging.

Consistency and Reliability:
Meeting the Requirements of Mass Application

The application of 100% offline dynamic compensation technology ensures the batch consistency of the Dhips^{+} series. Sampling tests on mass-produced products show that the accuracy error difference of the same model product under the same working condition is less than ±0.05%, which is crucial for batch application scenarios such as industrial production lines and new energy vehicle manufacturing that require a large number of deployed sensors.

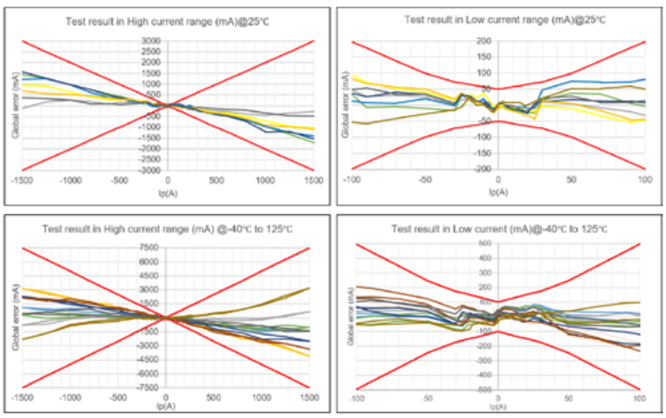


Figure 5: Full Temperature Accuracy of Dhips^{+} Series Products

It can reduce the difficulty of system debugging and improve the stability of the overall system.

Dhips+ Product Functional Safety: Safety Line for BMS Current Monitoring

As a core function of BMS, current monitoring accuracy and reliability are the keys to prevent battery overcurrent thermal runaway. The Dhips+ product launched by Innosense takes ASIL D level safety design as the core and builds a full-link functional safety guarantee system, providing a highly reliable solution for electric vehicle BMS current monitoring.

Product Name	Outline	Description	Busbar size	Continuous current (A) *	Peak current (A)	Functional safety	Output
BBA		Single Hall	20*3	350	1000+	ASIL C	CAN
BBB		Dual Hall	36*4	800	1500+	ASIL C/D	CAN
BBC		Dual Hall	46*5	1200	2000+	ASIL C/D	CAN
B1A/B		Single/Dual Hall	24*6	800	1500+	ASIL C/D	CAN
B1C		Single Hall	20*6	350	1000+	ASIL C/D	CAN

Figure 6: Parameters of Dhips+ Series Products

Core Objectives of Functional Safety
The functional safety design of the Dhips+ product takes solving the thermal runaway risk caused by battery overcurrent as the core objective. To this end, Dhips+ has established clear safety goals: preventing thermal runaway caused by overcurrent of the power battery system, with a Safety Integrity Level ASIL D level. The product strictly complies with the "Fault Tolerant Time Interval (FTTI)" requirement in standard. At the same time, the product design is fully aligned with the ISO 26262 standard and certified by the authoritative SGS organization to ensure full-process compliance in functional safety management, hardware design, software development, etc.

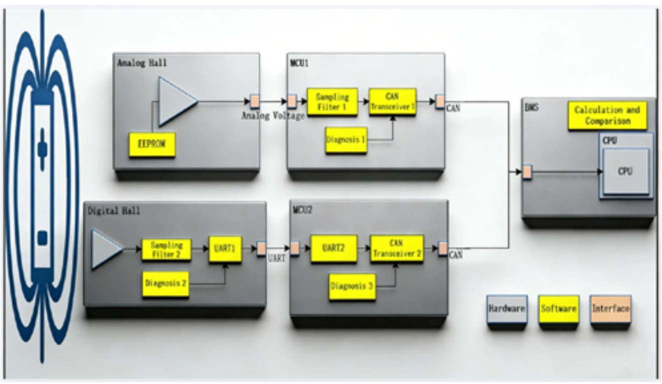


Figure 7: ASIL D SF Architecture of Dhips+ Series Products

Functional Safety Hardware Architecture
The Dhips+ product adopts modular hardware architecture and provides a functional safety level ASIL D configuration scheme. Through hardware redundancy and fault-tolerant design, it maximizes the reduction of random hardware failure risks. In the ASIL D hardware architecture, the Dhips+ product is equipped with a fully redundant architecture of "dual sensing channels + dual MCU processing + dual communication links".
Through the hardware heterogeneous design of "analog Hall + digital Hall" and software collaborative diagnosis, it builds a current monitoring safety barrier that meets ASIL D level requirements, perfectly adapting to the harsh requirements for safety redundancy in complex application scenarios such as 800V high-voltage platforms and fast charging.

Enterprise Strength: Innosense's Technical Accumulation and Innovation Philosophy

The successful launch of the Dhips+ series is inseparable from Innosense's long-term technical accumulation and continuous innovation spirit in the field of Hall sensors. As an enterprise focusing on the R&D and production of high-accuracy sensors, Innosense takes "reshaping the value curve" as its core philosophy and is committed to breaking the inherent industry balance through technological innovation and providing customers with higher-value product solutions.

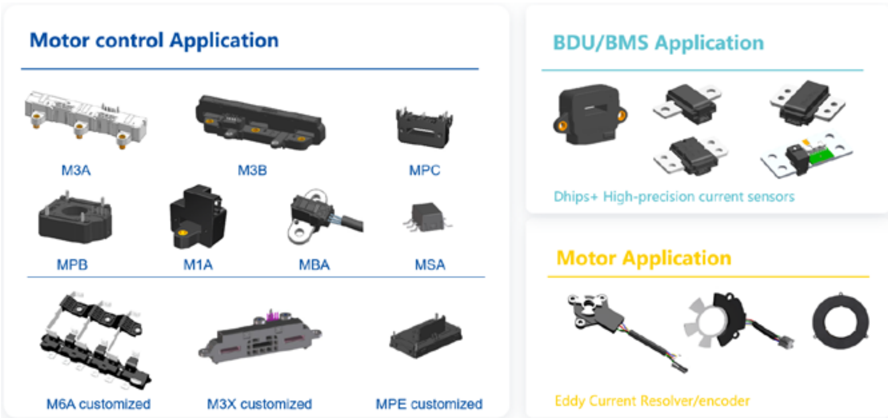


Figure 8: Partial Product Applications of Innosense

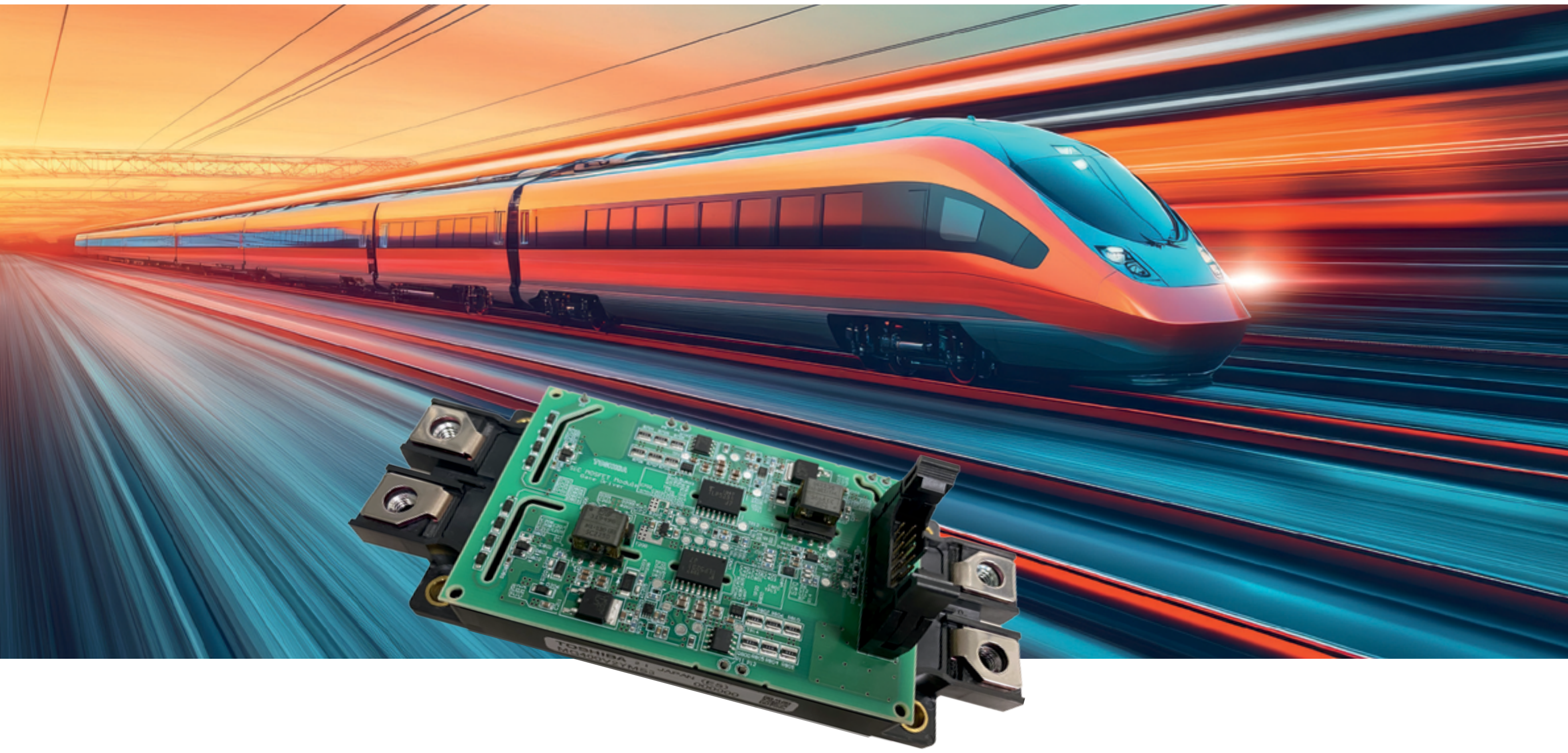
The company's global product team has profound industry experience and technical strength and a number of core technical reserves in system applications, algorithm development and other fields. Through in-depth cooperation with end customers, Innosense accurately grasps the pain points of market demand, conducts targeted technological R&D, ensures that products can effectively solve practical problems in applications, and reflects product value. Every link of the Dhips+ series products, from initial product design to the development of compensation algorithms, to the polishing of mass production processes, has undergone strict testing and verification to ensure the performance reliability and batch consistency of the products.

Conclusion: Outlook of High-Accuracy Sensing Technology
As the "eyes" of power electronic systems, the accuracy and reliability of current sensors directly determine the upper limit of system performance. The launch of Innosense's Dhips+ series high-accuracy Hall current sensors not only solve the technical pain points of traditional products, but also reshapes the industry's value curve, providing a cost-effective solution for high-accuracy current detection, and promoting the technological upgrading of new energy vehicles, industrial control, new energy power generation and other fields.

www.innosense.com

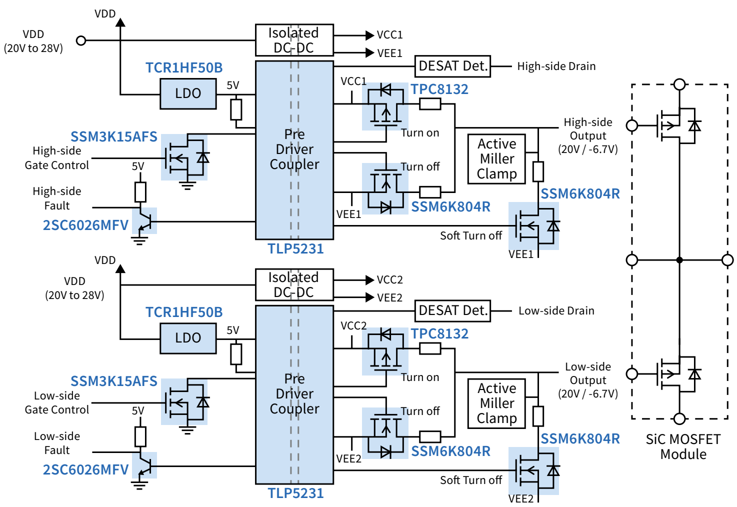
TOSHIBA

Gate Drive Circuit Solution for SiC MOSFET Module



Highlights

- Built-in implementation on a SiC MOSFET Module
- Output voltage +20V (typ.) / -6.7V (typ.)
- Output current ±9.8A (max.)
- Max. PWM frequency 50kHz
- Independent open-collector fault signal output of high-side and low-side



Featured Products

- **TLP5231** – isolated pre-gate driver
  - Split output
  - Fault signal feedback
  - UVLO protection
  - Soft shutdown
  - Over current protection using DESAT
  - Active Miller clamp
- **SSM6K804R** – n-ch MOSFET
  - 40V, 18mΩ @V_{GS} = 4.5V, 1.5W, TSOP6F package
- **TPC8132** – p-ch MOSFET
  - -40V, 20mΩ @V_{GS} = -10V, 1.9W, SOP-8 package
- **TCR1HF50B** – LDO Regulator
  - V_{IN}=4~36V, V_{OUT} = 1.8V to 5.0V, V_{OUT} = ±1% (T_a = 25°C)
  - Overcurrent protection, thermal shutdown, inrush current reduction
- **SSM3K15AFS** – n-ch MOSFET
  - 30V, 3.6Ω @V_{GS} = 4V, 100mW, SOT-416 package
- **2SC6026MFV** – npn transistor
  - 50V, 150mA (max.), SOT-723 package

https://toshiba.semicon-storage.com

Solving DC/DC Power Challenges in Military Avionics Through Modularity (Part 4)

While the first three episodes detailed military and avionic standards and front-end solutions, this last part 4 delves into the core of energy conversion. Part 4 will examine the critical challenge of selecting the optimal DC/DC converter topology and mode of operation, tackle magnetic circuit design, and address auxiliary functions and reliability concerns. Finally, this story will outline a comprehensive modular power architecture, built from the functions previously discussed and realized through specific COTS modules. PCB layout considerations will also be discussed.

By Christian Jonglas, Technical Support Manager, GAIA Converter

Designing a full DC/DC converter with discrete components is definitively the most complex, time-consuming, and risky approach. Consequently, engineers who choose this path probably have compelling reasons. Sometimes the required specifications aren't available in Commercial Off-The-Shelf (COTS) products. Other times, the form factor of a COTS DC/DC converter – despite offering better power density – doesn't fit the customer's needs, or the designer requires a unique function unavailable in COTS solutions. For engineers opting for a discrete design believing it will outperform a COTS-based solution or hoping to master component procurement, it is paramount to carefully balance the risks and benefits.

The multi-phase design process itself presents significant challenges in terms of topology choice, magnetics & switching component selection as well as control loop and protections.

Topology Choice

The choice of topology is a critical decision which requires a highly skilled power supply designer. For example, selecting a flyback topology for low-power isolated DC/DC converter leverages its low component count, which improves reliability through higher MTBF figures. To simplify design, engineers may choose Continuous Conduction Mode (CCM) operation. However, CCM demands a larger transformer with a correctly rated air gap to prevent core saturation, and an accurate output voltage control for limiting the light loads voltage raise. Conversely, Discontinuous Conduction Mode (DCM) yields a smaller transformer size and more stable light-load voltage regulation—at the expense of higher ripple current that increase components stress lowering the MTBF.

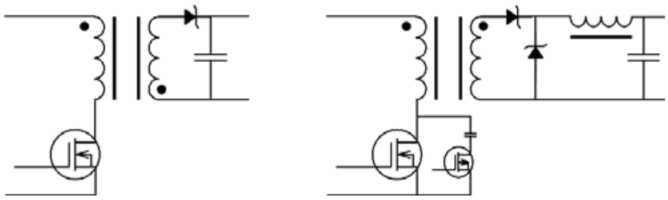


Figure 1: The flyback topology, with its low component count and a single magnetic circuit that provides both isolation and energy storage, is ideal for achieving high MTBF. The forward topology using a transformer for isolation and a separate power inductor for energy storage is essential for high powers.

Magnetics & switching component selection

Success demands expert knowledge of state-of-the-art market offerings. The limited availability of branded off-the-shelf transformers often forces engineers to adapt designs to magnetic specifications, compromising circuit flexibility and performance. Opting for custom transformers entails extended design cycles, including iterative development and qualification phases. ACR (resistance in alternative current mode) and DCR (resistance in direct current mode), key contributors to transformer efficiency, cannot be taken as simple figures from off-the-shelf transformer datasheets. Instead, they require accurate evaluation through complex computations prior to design, followed by verification on initial prototypes.

Control loop and protection

Following core power stage definition, comprehensive design of low-power support electronics is essential. This encompasses the regulation control loop, critical safety/protection functions (Under-Voltage Lockout - UVLO, Over-Current Protection – OCP, Over-Voltage Protection – OVP), and auxiliary features such as switching frequency synchronization, remote control, and monitoring.

Design considerations extend beyond functionality. In this context it is important to consider reliability considerations as well as component obsolescence & sourcing.

Reliability considerations

Although opto-coupler-based analog feedback loops are simple, their inherent reliability issues make them unsuitable for demanding military and avionics applications. A more robust solution uses a discrete magnetic feedback circuit, which transmits error signals through a low-power transformer. This design offers high MTBF and superior dependability, despite its greater complexity.

Component obsolescence & sourcing

Proactively managing component availability and obsolescence demands significant resources. Ensuring manufacturability over extended lifecycles (10-30 years) requires implementing multi-sourcing strategies and monitoring component change notifications during the initial design phase. As electronic specialists most design engineers underestimate the technical and financial constraints associated with preventing obsolescence.

COTS Converter

With a comprehensive range of DC/DC board converters covering power needs from 4 W to 1000 W, Gaia Converter has spent the last three decades working on power conversion technologies. Today, the company offers several Hi-Rel COTS board-mounted DC/DC converters. Its low-power DC/DC converters (6–80 W) combine CCM and DCM operation to extend input voltage range boundaries without efficiency compromise, while quarter-brick and half-brick converters (155–500 W) leverage a copper IMS (isolated metallic substrate) base construction to avoid power derating at high temperatures. Gaia Converter's proprietary magnetic feedback technology, introduced years ago, extends the lifecycle of these high-power-density converters by eliminating drift risks inherent in opto-coupler feedback control loops.

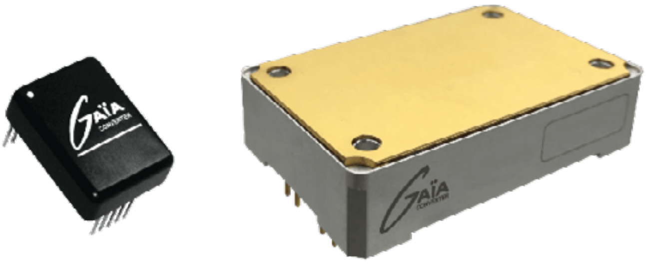

Are wide-bandgap switches still
too fast for your HIL simulator?
Have no fear, the
RT Box is up to the task.
High fidelity controller HIL testing,
even when switching at 1 MHz.
www.plexim.com/nanostep
plecs
RT Box 3
plexim
electrical engineering software

COTS REF.	MGDM04/10/18	MGDD8/21/40/80	MGDM75/100	MGDM155/250	MGDM500	MGDM500/P
parameters						
output power	4 /10/18	6/8/20/40/80	75 /100	100/250	500	500 to 3000
Output number	Up to 3	2	1	1	1	1
Wide input	4:1	9:1 to 12:1	5:1-10:1	5:1	5:1	5:1
Output voltage	3.3 to 24	3.3 to 54	3.3 to 28	3.3 to 28	12 to 48	12 to 48
synchronization	No	Yes	Yes	Yes	Yes	yes
MTBF (Hours)	1650 000	1025000	600000	490000	1724000	1724000
package	DIL	1/8 Brick to 2"x1.6"x0.5"	¼ Brick	¼ Brick	½ Brick	½ Brick

Table 1: Modular approach allows flexibility with available power from 4W to 500W +, and input range from 4:1 to 12:1.

Power architecture

Considering all mandatory functions for building a Mil-Aero compliant power supply, a COTS-based modular approach appears remarkably straightforward. Leveraging COTS solutions provides designers with simplified development processes and accelerated qualification timelines. The power designer's responsibility reduces to implementing the module arrangement detailed in Gaia Converter's application notes [4.1], adapting them to specific requirements.



8W Isolated COTS DC/DC converter 250W Isolated COTS DC/DC converter

Figure 2: The 8 Watts 1/16th brick and 250 Watts 1/4 brick COTS isolated DC/DC converters are compact board mounted modules.

PCB Considerations

However, project success depends on the engineer's ability to design a state-of-the-art PCB for module interconnections. While COTS modules greatly simplify design, the PCB layout demands specialized skills to avoid compromising performance despite module quality. Fundamentally, when routing copper traces, designers must address at least five key questions:

1. How resistive will my copper trace be? (and consequently, what will its temperature be during operation).
2. How inductive will the copper trace be?
3. Will radiated energy quickly find a return path?
4. Will the routed trace favor undesired signal coupling between points?
5. Will creepage and isolation distances comply with requirements?

The answer to Question 1 lies in selecting the correct compromise between trace width and copper thickness. Answers to Questions 2 and 3 are addressed in Figure 3, where example 1 shows how an inductive thin trace can transform a low-impedance common-mode capacitor into a resonant LC circuit, while example 2 highlights the benefit of keeping a positive power track and its return path as close as possible to minimize radiated noise (radiated field lines shown in yellow). These simplified examples of good and bad practices use single-layer routing for clarity.

Utilizing multilayer PCBs and smart copper plane use are key elements that help the power supply PCB designer follow these best practices and ensure project success. Gaia-converter supports engineers in their PCB designs and offers fully documented demo boards examples. Figure 4 illustrates a 500 W power supply compliant with Mil-Aero standards – an exceptionally simple architecture built around four proven high-reliability modules and described into Gaia-converter GTJ2050 service-manual [4.2].

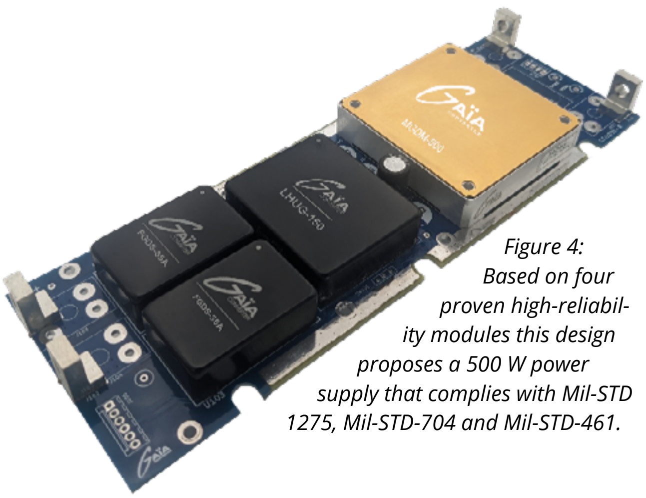
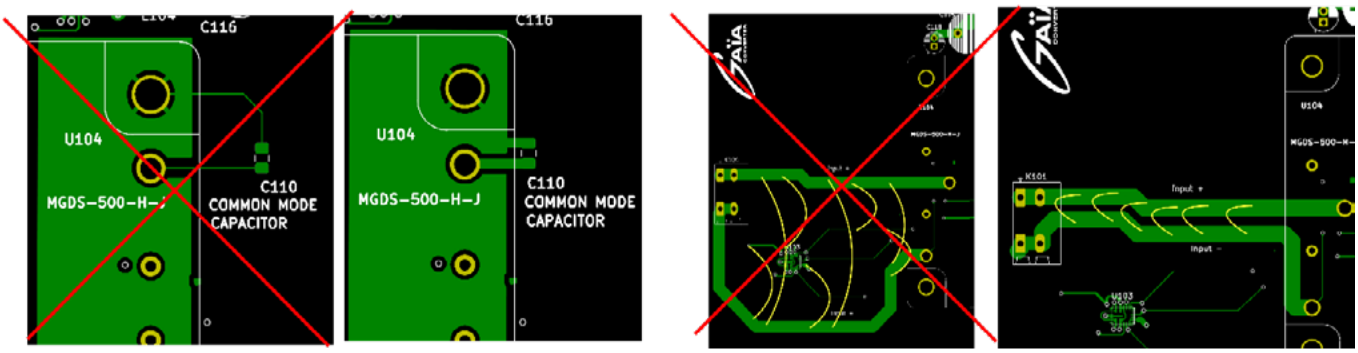


Figure 4: Based on four proven high-reliability modules this design proposes a 500 W power supply that complies with Mil-STD 1275, Mil-STD-704 and Mil-STD-461.



Example 1 *Example 2*

Figure 3: Traces that are too thin are inductive and cancel out the c110 effect (Example 1). Radiated field lines (in yellow) must be contained to avoid polluting secondary circuits in Example 2.

For lower-power solutions, further simplification is achievable. The fully integrated FLHG-60-MN front-end module incorporates EMC filtering, voltage limiting, reverse polarity protection, and hold-up functionality. As this single module ensures full compliance, only two components are required to construct a high-reliability Mil-Aero power supply. This 2”×3” solution examplifies SWaP optimization. Extending this integration trend, Gaia Converter recently released the board-mountable PSDG48 module – consolidating all architectural functions within a single package.

Figure 5: The 3.5”x3.30” 40 W power supply complies with Mil-STD-461,Mil-STD-704 and DO-160 with hold-up function thanks to the FLHG-60-MN integrated front end.

Conclusion

Engineers developing electronics for military or avionic applications often face demands for more complex digital, radio communication, and automated systems, resulting in soaring power consumption. However, as specialists in their domain they may lack full understanding of military and avionics standards, leading them to underestimate the challenges of developing compatible power supplies. For engineers without Mil-Aero power expertise, attempting to design a discrete-component power supply can be misleading and ultimately undermine the entire project: the design might pass demanding standards like DO-254 and DO-178, but fail MIL-STD-461 or DO160 compliance due to power supply issues. Designing mil-aero power supplies can quickly become a titanic undertaking for non-specialists. For over 30 years, Gaïa Converter has offered qualified, hi-rel, board-mounted power modules that greatly simplify mil-aero designs.

References:

[4.1] https://www.gaia-converter.com/technical-support/evaluation-boards/
[4.2] https://www.gaia-converter.com/wp-content/uploads/2025/08/GTJ2050-C_service_manuel_Rev-B.pdf
[4.3] https://www.gaia-converter.com/products/lgds-600/
[4.4] https://www.gaia-converter.com/products/mgdm-500/

www.gaia-converter.com

Thermal Management for SiC Semiconductors – Top Side Cooling as an Innovative Solution

The growing demand for powerful and compact power electronics places high demands on the thermal management of modern semiconductor technologies. Silicon carbide (SiC) and gallium nitride (GaN) semiconductors in particular offer significant advantages over conventional silicon solutions, including higher voltage resistance, lower switching losses, and improved efficiency at high temperatures. However, this higher power density is accompanied by increased cooling requirements.

By Wolfgang Höfer, Business Management Leader Thermal Management, Kerafol

Traditionally, heat dissipation occurs via the underside of the semiconductor (bottom side cooling), whereby the heat loss is transferred to the housing through the substrate and the solder joint. However, multiple thermal interfaces limit the efficiency of this method. Top side cooling is a promising alternative, in which heat is dissipated directly to a heat sink via the top of the chip. This reduces thermal resistance and improves temperature homogeneity within the semiconductor, which in turn increases the service life and efficiency of the entire system.

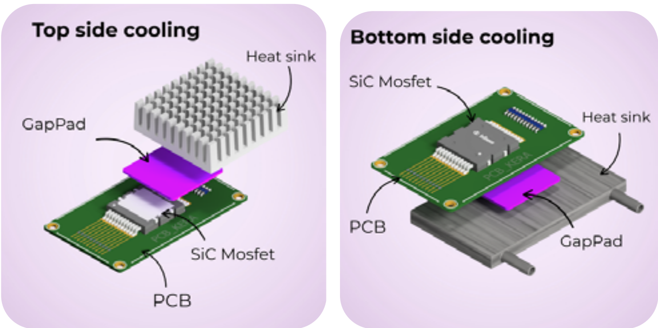


Figure 1: Bottomside vs. Topside Cooling

A key factor for the successful implementation of top side cooling is the selection of a suitable thermal interface material (TIM) that enables efficient heat transfer.

Challenges of conventional TIMs for top side cooling
To optimize heat dissipation in top side cooling, TIMs must meet several requirements: They should have high thermal conductivity, minimize thermal resistance, provide electrical insulation in most applications, and offer high mechanical stability and reliability.

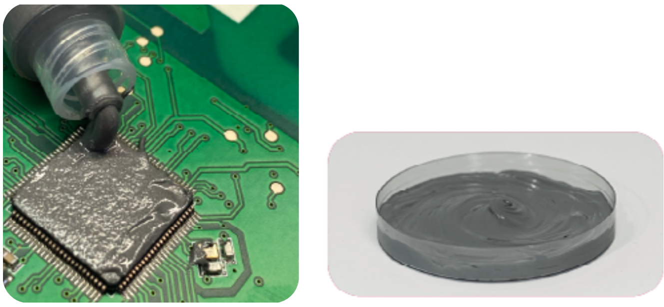


Figure 2: KERAFOL® KP 100

Due to their low bond line thickness (BLT), thermal greases have very low thermal resistance, but they are not electrically insulating. Some of the greases available on the market also tend to exhibit the so-called "pump out effect," especially during more intensive power cycles. The KP100 was specifically developed to significantly reduce the "pumpout effect". In general, applying paste using screen or stencil printing is very time consuming. Pastes are also not intended for tolerance compensation; cross-linking systems such as gap filler liquids are used for this purpose.

Phase change materials (PCM) melt at higher operating temperatures, thereby reducing their contact resistance. However, they tend to be mechanically unstable over a longer period or over a higher number of cycles and can therefore lose performance. This material group is also not suitable for applications requiring electrical insulation. In addition, application of PCM requires special time-consuming assembly methods such as screen printing.

Figure 3: KERAFOL® PCM

Figure 4: KERAFOL® GFL 3030

- **The use of gap filler liquids** has become a popular solution, especially for l quantities. The combination of high thermal conductivity, low material costs, and easy automation using dispensing systems offers lots of advantages here. Unlike the product groups mentioned above, gap filler liquids are also electrically insulating. The disadvantage here is the longer processing time in production due to the necessary cross-linking process of the material itself. In the case of complex geometries, the exact control of material distribution is somewhat more difficult due to the dependence on the dispensing process and component tolerances. Nevertheless, gap filler liquids are a very popular choice because they offer great advantages in tolerance compensation due to their "wet-on-wet" installation, and the mechanical pressure on the assemblies is very low.
- **KERAMOLD** is a specially developed, thermally highly conductive, and electrically insulating granulate based on TPE, which combines the advantages of various material groups in the field of TIMs. It is applied directly to the circuit board or semiconductor chip in the overmolding process, creating a precisely fitting, thermally conductive, and electrically insulating protective layer, all without a cross-linking process.

Exkurs Hybridfolie

The trend (e.g., in the automotive industry) towards 800V architecture instead of the previous 400V poses new challenges, particularly in the area of electrical insulation strength. For safety reasons, a 2-layer TIM structure is required, for example, to ensure electrical insulation even in the event of contamination by metallic particles or air pockets. There are various possible combinations here, which are discussed in more detail in a separate application note entitled "Thermal management for SiC semiconductors in the 800V range: Top side cooling with hybrid foil."

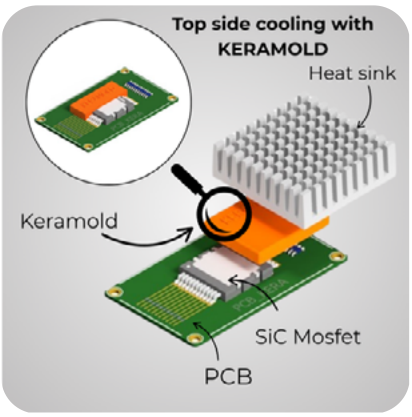


Figure 5: Topside Cooling with KERAMOLD® 15

One option is to use a combination of thermal conductive film and gap filler liquid. Both layers are electrically insulating and thermally conductive, and the gap filler can be used to compensate for component tolerances. An alternative approach is to use a specially developed ultra-thin ceramic, which is still flexible and highly electrically insulating (approx. 5kV) with a layer thickness of only 40 µm.

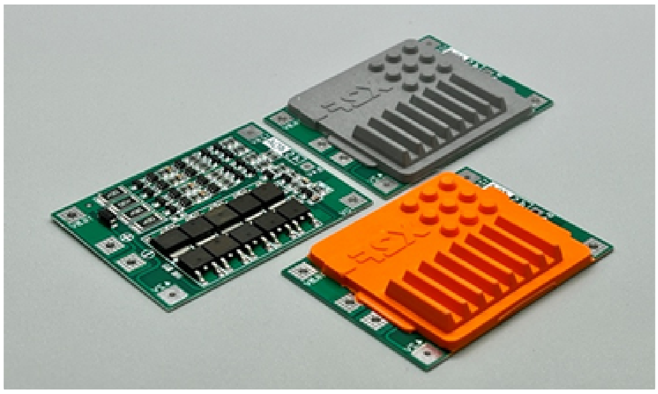


Figure 6: KERAMOLD® umspritzte Platine

Areas of application for top side cooling with KERAMOLD

Top side cooling in particular poses a number of mechanical, electrical, and thermal challenges. The heat dissipation of the SiC semiconductor consists of conduction and switching losses and, depending on the application, can amount to several hundred watts per module (e.g., in SiC MOSFETs for inverters in the EV industry). In addition, the requirements for insulation strength are also increasing; the electrical insulation of the TIM often has to be several kV, but this can be achieved with KERAMOLD material.

The overmolding process minimizes the contact resistance between the KERAMOLD material and the semiconductor. The high softness and elasticity of the KERAMOLD material, which, unlike conventional plastics, is in the low Shore A range, also contributes to this.

Figure 7: KERAMOLD® 15

ADVANTAGE	EFFECT/BENEFIT
HIGH THERMAL CONDUCTIVITY	Efficient heat transfer from the chip to the cooling surface
STANDARD FIT	3D parts and precisely fitting encapsulation of components possible
ELECTRICAL INSULATION	High insulation resistance (protection against short circuits)
AUTOMATIONCOMPATIBLE	Reduction of process time and material usage

High thermal conductivity: Thanks to special fillers, products in the KERAMOLD range achieve a thermal conductivity of over 2.5 W/mK in the z-direction (through plane) and over 3.2 W/mK in the x/y direction (in plane), which is also significantly higher than conventional plastics. A material with 3.5 W/mK (KERAMOLD 35) is already in development. Improved heat dissipation and additional heat spreading allow hot spots to be cooled moreeffectively and, if necessary, heat sinks to be made smaller.

Precise fit: The 3D shape of the TIM not only improves heat transfer itself but also makes it easier to deal with creepage currents, as not only the contact surface of the semiconductor but also, for example, the pins are connected and encapsulated. Material utilization is also very high with this method and can be reproduced. KERAMOLD has a CTI of > 600V, which means it can be classified as insulation class I and can help to keep component spacing small.

Excellent mechanical strength: Overmolding with soft and elastic TPE provides additional protection for the semiconductor chip against mechanical stresses such as vibrations or CTE mismatch, moisture, and environmental influences, which extends the service life of the electronic components.

All-in-one solution: Thanks to the complete encapsulation of the circuit board and the SiC semiconductors, other materials and process steps such as potting or conformal coating are no longer necessary, as the KERAMOLD material was developed not only for heat transfer but also for protection of the electronic assembly.

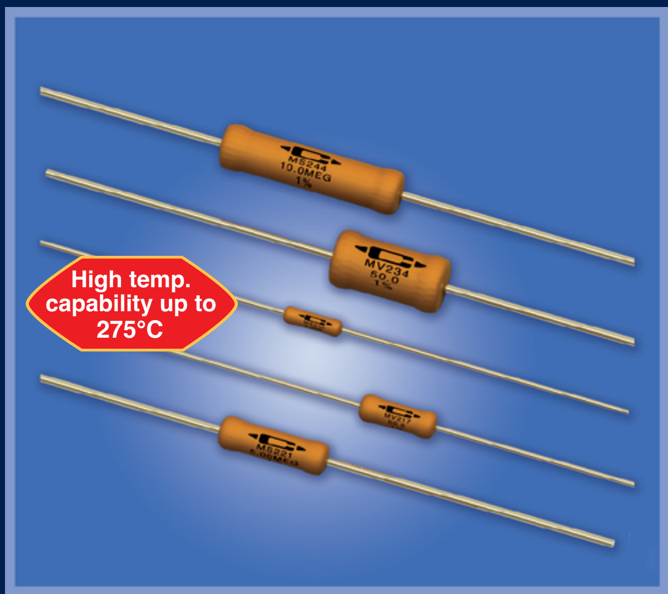
Figure 8: KERAMOLD® 25

Conclusion:
KERAMOLD as a key technology for efficient top side cooling The requirements in the field of power electronics are very complex and individual. Therefore, it is not possible to say in general terms which TIM group should be used, as this depends on many factors.

Nevertheless, KERAMOLD definietely represents a new approach here and gives developers new degrees of freedom.

By directly overmolding the semiconductor with a thermally conductive protective layer, considering a reduced process time in the manufacturing, heat dissipation, electrical insulation, and mechanical stability are all optimized. The KERAMOLD product range shows its greatest advantage when, in addition to protecting the electronics, an improvement in thermal performance is also required. The performance of KERAMOLD can and will be further improved, which is still necessary for some applications.

www.kerafol.com



Resilient Battery Energy Storage for Renewable-Rich Grids

Today's power grids increasingly depend on decentralized energy sources such as solar and wind. Because their generation fluctuates, Battery Energy Storage Systems (BESS) have become essential for grid stability. Grid-supporting BESS must comply with strict requirements for performance, functional safety, and cybersecurity.

By Muhammad Fawwad, Product Marketing Manager, Moxa Europe

A modern utility-scale BESS typically integrates battery modules with Battery Management Systems (BMS), a bidirectional Power Conversion System (PCS), and an Energy Management System (EMS) that optimizes operation and ensures compliance with grid requirements.

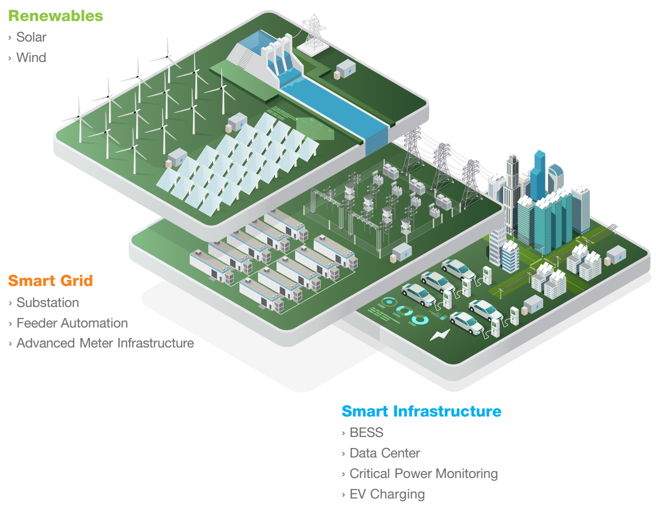


Figure 1: Battery energy storage plays a pivotal role in modern power systems when strict requirements are met.

Grid-connected BESS must meet binding obligations for frequency control, voltage support, and ramp-up behavior. In ancillary-services markets, operators must prove that their systems can reach full active-power output within defined time windows. For example, participation as frequency reserve may require sub-second response, while manual frequency restoration allows minutes. Meeting the specified ramp-up speed is both a contractual requirement and a technical safeguard for grid stability; non-compliance risks market exclusion and undermines system reliability. Ensuring predictable, high ramp-up performance becomes a critical design goal and is directly linked to power-electronics capability, built on the solid foundation of a resilient communication network.

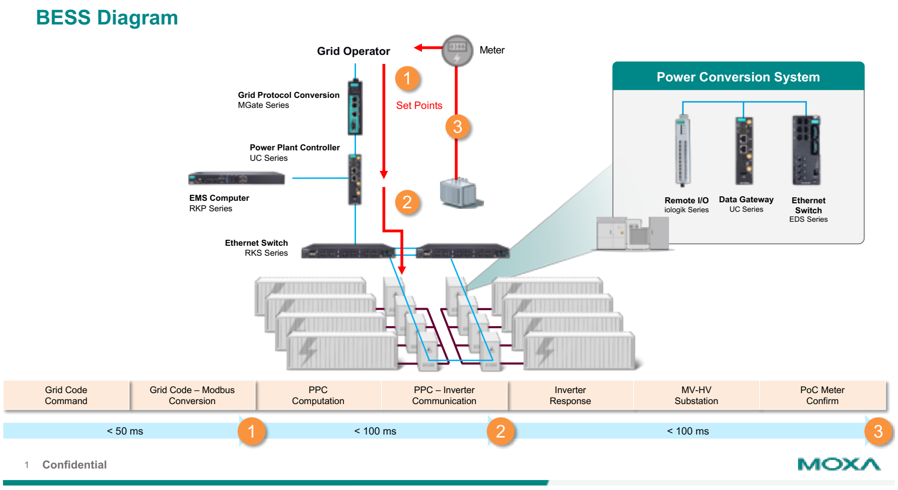


Figure 2: Tight time budgets: 1) TSO sends set-point to PPC; 2) PPC configures inverters; 3) System status back to TSO.

Digitalized Communication and Deterministic Control

BESS are scalable systems whose overall power and energy are achieved by multiplying PCS and BMS elements. These components communicate with each other, with the EMS, and with external parties exclusively via IP-based digital communication. As in other parts of the power sector, the IEC 61850 standard is increasingly used to ensure interoperability.

Typical embedded protocols include:

- **GOOSE** for ultra-fast event messaging for protection
- **MMS** for supervisory control and configuration

BESS networks, and their connections to external networks with IEDs (Intelligent Electronic Devices) and Power Plant Controllers (PPC), should prioritize traffic. IEC-61850-oriented devices and configurations enable deterministic end-to-end behavior. However, protocols alone cannot deliver fast, coordinated power ramp-up. A consistent supervisory control layer must synchronize responses across the entire BESS. When the grid operator issues set-points, this controller distributes commands simultaneously to all inverters, preventing uneven responses and potential oscillations. Technically, it requires low-latency communication, secure and fault-tolerant operation, and long-term reliability under demanding conditions, forming a deterministic communication backbone that translates grid signals into synchronized inverter actions and predictable power availability.

Network Resilience and Topology Design

Even with capable power electronics and protocols, ramp-up compliance ultimately stands or falls with the underlying network topology. A single point of failure can add reconvergence delays of seconds, which is enough to miss grid-code windows. Resilient topologies such as Turbo Ring and Turbo Chain provide recovery times under 50 ms, while PRP/HSR enables zero-loss redundancy for seamless communication during faults. These approaches ensure inverter commands and measurements continue to flow, even if links fail while set-points are being executed. Recovery times remain well below expected service intervals (see Figure 2).

Selecting a topology requires balancing cost, scalability, and compliance: Turbo Ring/Chain is a cost-effective choice for PCS networks, while PRP is ideal for zero-switchover redundancy in substations.

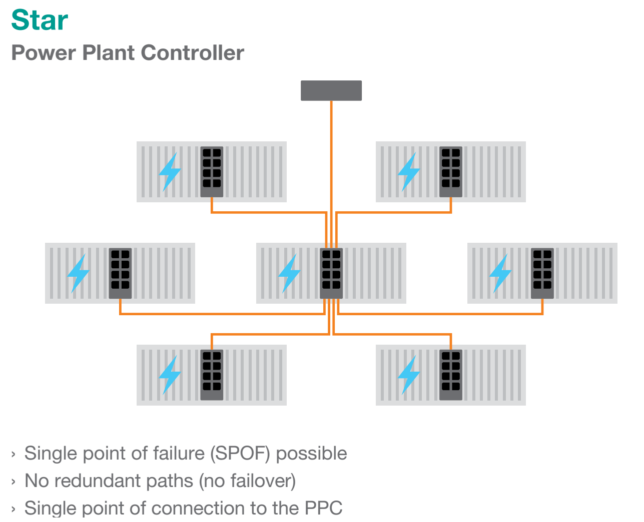


Figure 3: The right topology determines achievable recovery times.

Figure 4: MxView with the MxSecurity module helps operators protect their networks.

In all cases, highly available networking is what enables the short ramp-up times demanded by modern ancillary-services markets, turning the network from a passive utility into a strategic enabler of long-term grid stability.

Cybersecurity in BESS Networks

System resilience today is more than robust hardware. Unsecure firmware and software can expose latent vulnerabilities that allow unauthorized access or data exfiltration. For OT engineers and compliance officers, maintaining command and control requires resilient connectivity and a proactive cybersecurity posture. Frameworks such as IEC 62443 and NIS2 guide organizations in embedding security across operational layers. Moxa supports these standards with the MxView network-management platform and its MxSecurity module. The platform visualizes device-level security configurations and provides actionable recommendations based on Zero-Trust principles, helping teams harden their networks against evolving threats.

Moxa hardware, particularly the EDS-4000, PT, and MDS switch families, also integrates key security features, including:

- Port Rate Limiting & Port Lock to block unauthorized traffic
- Authentication & Trust Access Control to verify and manage access
- Access Control Lists & MAC Sticky to enforce device-specific policies
- SNMP v3 for secure network-management communications

In addition, Moxa's logging supports forensic analysis and continuous hardening, serving as a reliable basis for security audits and compliance reporting.

Conclusion

Deploying BESS in modern grid infrastructures requires advanced engineering, robust communication protocols, and resilient system architectures. Deterministic responsiveness and high fault tolerance are decisive. Ethernet-based ring and PRP/HSR topologies deliver sub-second recovery in unfavorable cases and, at best, uninterrupted data flow, both essential for grid-code compliance and operational continuity. Cybersecurity frameworks such as IEC 62443 and NIS2 must be embedded at device and network levels to enable Zero-Trust architectures and proactive threat mitigation. The result is grid-connected BESS that not only satisfy stringent TSO requirements but also deliver measurable returns.

www.moxa.com

Smart GaN Buck Controller Designs - Part 1: Considerations and Measurements

Synchronous converters operate by alternately toggling a control switch and synchronous switch device (usually a FET) on and off. The timing of this operation matters. If the delay between turning one switch off and the other on is longer than necessary, efficiency suffers. If the delay is not long enough, a condition known as shoot-through can occur when massive amounts of current flow through the switch pair. This dramatically hurts efficiency and can damage components. Understanding the dynamics involved and how to properly measure them is discussed in this first of two articles about smart GaN buck controller designs.

By James R. Staley, Senior Product Applications Engineering Manager, Analog Devices

The introduction of wide bandgap FET devices such as gallium nitride (GaN) in power conversion offers higher energy density, faster switching, and lower losses due to their dramatically lower gate capacitance (Cg). GaN FETs, however, have very tight V_{GS} limits and do not have a body diode. Because of this, the reverse conduction losses are much higher with longer dead times if the gate slew rate is lowered to avoid gate ringing. But they are still just as subject to the deleterious effects of shoot-through. To take full advantage of these devices, dead time must therefore be optimized. Consider the typical application in Figure 1. This is a 15 V to 36 V_{IN}, 12 V/15 A step-down converter featuring the LTC7891. It is designed specifically for driving GaN devices, and we will examine how to accurately measure dead time and overshoot while optimizing the gate resistor using this application circuit.

Switching Operation Considerations

The switching network for the buck converter with smart near-zero dead time is comprised of the controller that drives control switch Q1 top gate (TG) and a synchronous switch Q2 bottom gate (BG). The top gate is driven with separate pull-up/pull-down resistors (TGUP, TGDN) and the bottom gate is driven with separate pull-up/pull-down resistors (BGUP, BGDN). Switching currents during each switch cycle are averaged with the output filter network L1 and C_{OUT} to produce a regulated output voltage.

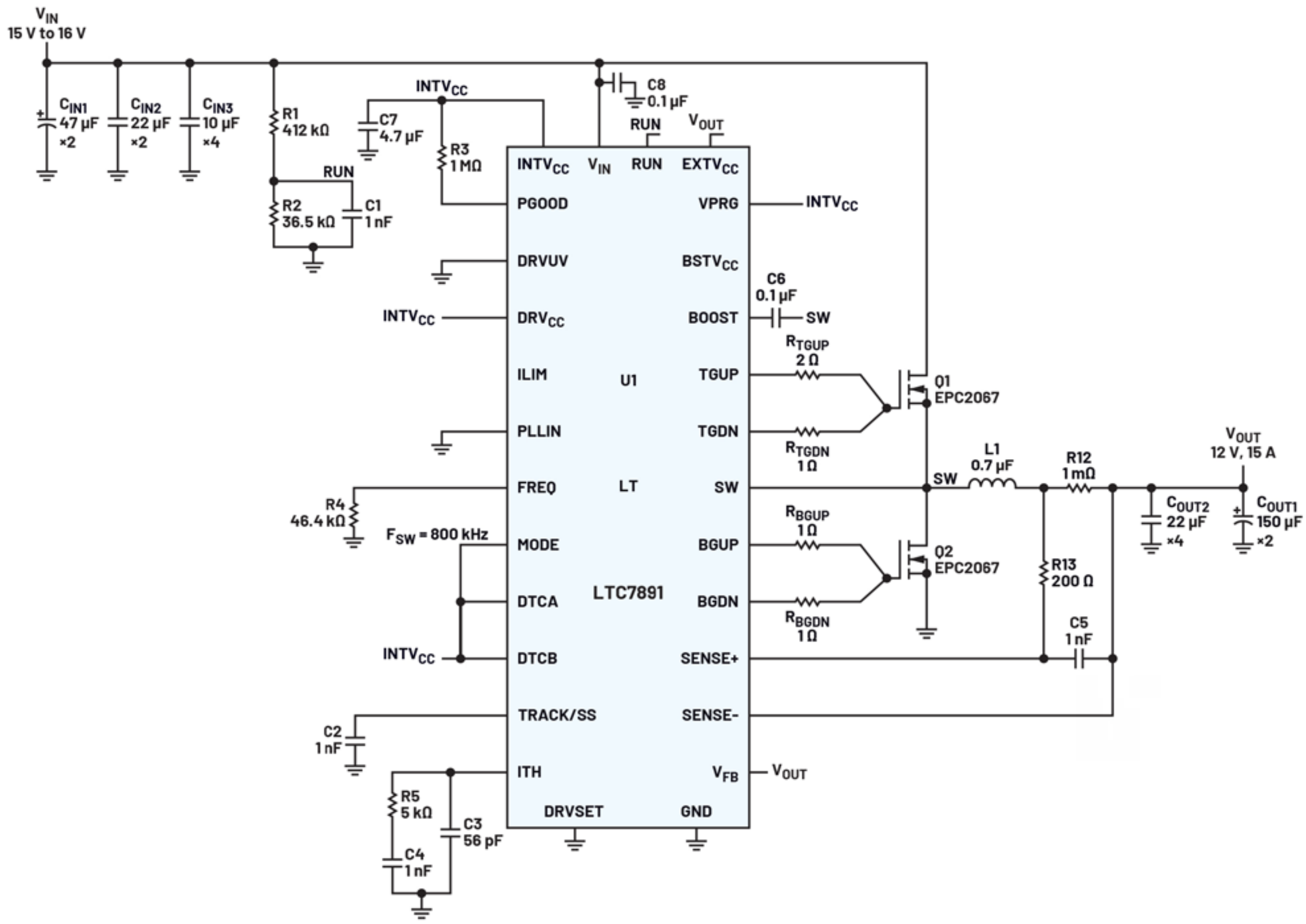


Figure 1: 800 kHz, 15 V to 36 VIN, 12 V buck regulator providing up to 15 A output.

An ideal converter would have lossless switches that turned on and off instantly in perfect unison. However, while GaN FETs are capable of being turned on and off more quickly than other technologies due to their low capacitance, there are delays between the controller commanding a switch on, and that switch reaching a fully on state. The same holds true for turning the switch off. Because of this delay, there are transition losses that become an important part of the total losses of switching operation. These losses translate into switch heat, which hurts efficiency and ultimately imposes thermal limits of operation for the FET. But how does one practically work with these limits imposed by nonideal switches?

If both switches are fully on - even for a fraction of a second - low $R_{DS(ON)}$ means a short circuit from V_{IN} to GND, and catastrophic switch failure is the result. If both switches are partially on, high drain currents cause instantaneous high temperature rises that stress the switches and reduce their lifetime. This condition is known as shoot-through (Figure 2). The initial switching has roughly

8 ns of dead time and the switch current has a normal di/dt associated with switching to input current, then ramping as the inductor charges. The next transition has symmetric rising and falling edges, allowing both transistors to be partially on and resulting in a sharp spike of drain current that is still below I(DS)MAX. The final transition allows 2 ns of on-time overlap and the drain current spikes well beyond the rated FET drain current.

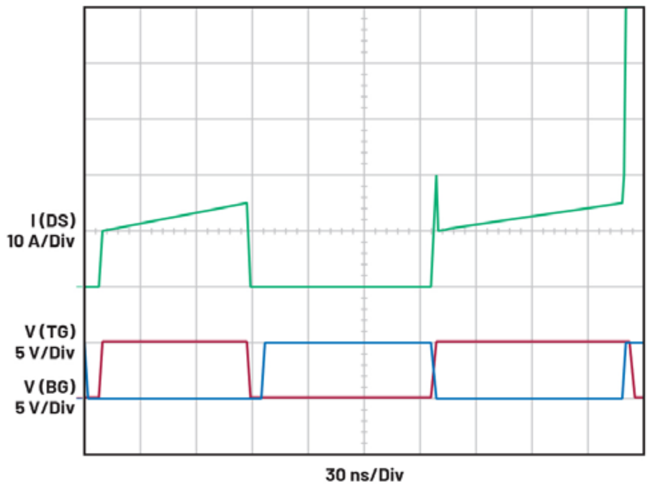


Figure 2: Shoot-through caused by insufficient dead time.

To avoid this, controllers turn one switch off and then delay the turn-on of the other, which is a period known as dead time. This prevents shoot-through only if the programmed dead time is sufficient to allow the transition from completely on and off (Figure 2). But what happens if this time is too long? MOSFETs have a parasitic body diode that will clamp the switch node and prevent reverse breakdown while the FET is still off. This temporary VF × IDS power loss eats into efficiency the longer it takes for the FET to turn fully on and replace the (typically 0.8 V to 1.0 V) VF × IDS power loss product with the IDS2 × $R_{DS(ON)}$ loss, which is much lower. GaN FETs, on the other hand, do not have this body diode structure. They will clamp under reverse voltage at a much higher potential, with 2 V typical for the lateral transistor structure. This means that excessively high power losses will be incurred for even moderate dead times, making it essential for GaN FET controllers to minimize dead time. To overcome this, MOSFET-based designs often place a Schottky diode across the synchronous switch in parallel with the MOSFET to reduce the forward voltage drop during dead time. The diode's junction capacitance, however, quickly dominates as a source of loss in the higher switching frequency applications GaN is ideal for. The trade-offs associated with these considerations are shown in Table 1.

	BSZ097N10NS5 MOSFET	EPC2218 GaN FET	PMEG100T030 Schottky
V_F (V)	0.9	1.5	0.7
I_D (A)	20	20	20
Reverse Conduction Loss (W)	0.36	0.60	0.28
Q_{RR} (nC)	60.0	0.0	9.5
Reverse Recovery Loss (W)	1.44	0.00	0.23

Table 1: Losses from 48 V to 12 V at 500 kHz F_{SW} and 20 ns Dead Time.

GaN-based designs are now seemingly between a proverbial rock and a hard place. Shoot-through from dead time failure and the switches instantly evaporate; too much dead time and they could de-solder themselves right off the board. How does one determine the right balance between efficient conversion and an adequate safety margin? Perhaps the easiest way to solve this dilemma is to choose a converter that offers smart near-zero dead times or adaptive dead time features baked into the silicon. The LTC7890 and LTC7891 step-down controllers are dual-/single-buck designs that are purpose built to drive GaN FETs with pin selectable smart near-zero, adaptive, and precision resistor adjustable dead time control options. The architecture cleverly measures the actual V_{GS} and V_{SW} levels to intelligently control timing to achieve both precision and safety for any device being driven. It does this by making rapid adjustments to control a precise amount of dead time. Instead of the traditional open-loop gate drive, the programmed dead time is adjusted on the fly to guarantee turn-on and turn-off occurs when the controller needs, rather than when the gate signal along with parasitic gate resistance and capacitances dictate. This minimizes the reverse conduction losses and capitalizes on the near-zero reverse recovery loss inherent to GaN. A complete guide to these modes of operation is shown in Table 2. All that is left for the user is to verify that the programmed mode and timing are implemented correctly. However, the verification process presents challenges the designer must first overcome.

Dead Time Control (DTC) MODE	DTCA	DTCB	Dead Time (ns)
Smart Near-Zero DTC	$INTV_{CC}$		0 (typ)
Adaptive DTC	GND		20 (typ)
RSET DTC	10 Ω to 200 kΩ	10 Ω to 200 kΩ	7 to 60

Table 2: DTC Mode Configuration.

Measurement and Layout Considerations

Measuring the dead time and overshoot waveforms requires careful attention to probing techniques and implementation. GaN FETs have very stringent V_{GS} constraints relative to MOSFETs - typically 5 V with +6 V to –4 V ABS_{MAX}. Strong gate drive with parasitic reactive elements leads to ringing, and even brief excursions can damage GaN devices. The GaN gate presents a lower capacitance to the drive pin than MOSFETs, which is what makes them compelling for use at higher frequencies. However, probes themselves present parasitic reactance elements that can distort the waveform and give incorrect information about what the gate sees unprobed. Holding a probe with the hand using minimal hardware can be an invitation for disaster should the hand slip. Using the traditional alligator clip lead is out of the question. Classically, custom pigtail application probing techniques have been recommended for good scope measurements, provided the return path is properly chosen for top gate and switch nodes (Figure 3). This still leaves the floating top gate with a problematic approach for probing. One solution is to use a connector such as the MMCX style, or header pins that will adapt to MMCX probe tips. While the bottom gate can be ground referenced, the topside gate is referenced to switch, so some form of isolated probe must be used. Optical probes, such as the Tektronix TIVP or newer TICP, which features less drift, can provide this isolation for the top gate measurement and utilize the MMCX connector. Figure 4 shows a typical LTC7891 dead time measurement setup in progress with the MMCX connector directly under the FET gate pin coupled to a 1 GHz optical probe.

The connectors themselves are a case study in compromise. Surface-mount MMCX connector placement can take up physical board space. This is a concern where very tight layouts for power density are an issue. If the connector is placed (optimally) directly across the gate and source pins of the FET without introducing additional gate trace, it may spread the layout more than desired. On the other hand, placing the connector out of the way of the layout introduces additional trace inductance and resistance that can degrade measurement accuracy. Another alternative is the use of hole-through headers that can be populated only for measurement and then left off for the final build, but this entails using an adapter that increases parasitic elements slightly, along with creating annulus space openings on all layers in the pad stack. With the optimum balance of trade-offs and careful attention to layout, a minimal amount of overshoot and ringing due to the probe parasitic elements can be achieved (Figure 5). The red outlined original layout had the MMCX connector solidly connected to the switch node and gate node connected with via and inner trace to the gate pad of the GaN FET. The red trace showed ringing exceeding +6.4 V/–9.1 V. Using the same 2.2 Ω pull-up/1.0 Ω pull-down gate resistance but modifying the blue outlined layout to separate the MMCX body from the switch node and Kelvin connect it instead, the blue trace shows +2.4 V/–1.8 V of ringing at the top gate turn-off. The key takeaway here is that even minor adjustments to the layout can have great impact on the measured overshoot figure, which is a key parameter for tuning out overshoot and ensuring that the GaN FETs are not being overdriven.

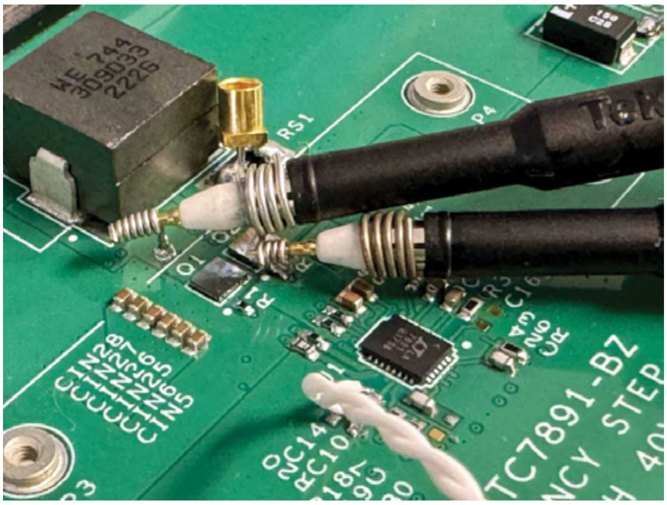


Figure 3: Good probing technique on bottom gate and switch to minimize ringing artifacts.

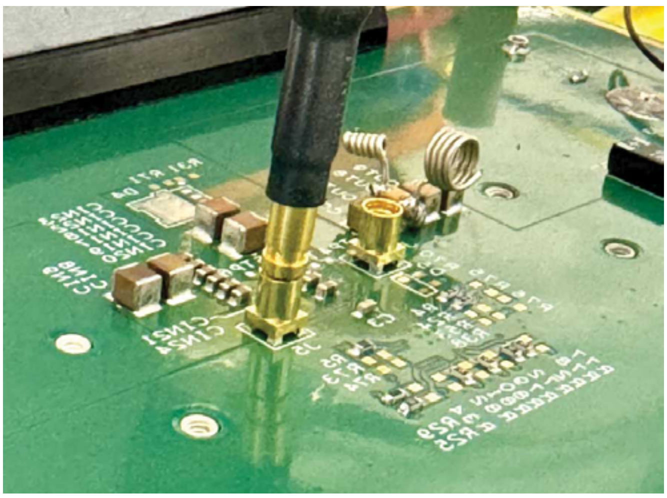


Figure 4: Tektronix TIVP100 optical probe connected to the top gate via an MMCX connector.

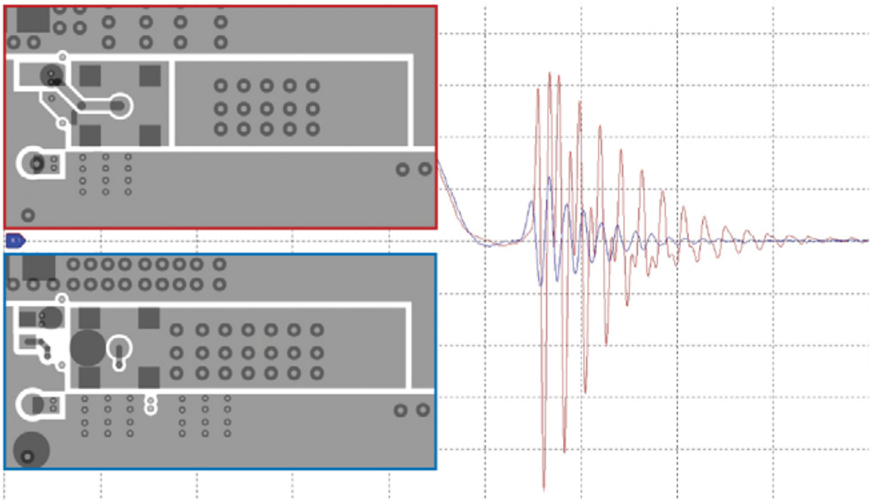


Figure 5: Top gate turn-off waveforms showing the effect of parasitic elements in probe connection. Red: non-Kelvin connected; Blue: Kelvin connected MMCX connector. 20 ns/div, 2 V/div using Tektronix TIVH 1 GHz optical probe.

Once the measurement technique is validated, the process of verifying dead time can begin. The first step is always to ensure that whatever type of probe being used to measure the top waveform is de-skewed with respect to the bottom signal using a common signal source. Dead time is relative, so the skew of one channel with respect to the other does not matter so long as a common signal shows up without any horizontal offset.

This also allows for ensuring that any gain error and offset (common issues with optical probes) are corrected for, or at least known for, post-measurement adjustment later. Optical probes should be allowed to thermally stabilize before collecting data that is used to make decisions. It is often useful to record any gain and offset settings.

About the Author

James R. Staley is a senior product applications engineering manager for Analog Devices. He graduated Eta Kappa Nu from North Carolina State University with a B.S.E.E. concentration in nanotechnology and has over 25 years of semiconductor industry experience. He has held positions with applications engineering, sales applications engineering, and systems engineering at Linear Technology and Analog Devices. His current focus is on industrial and precision instrumentation power systems. James and his family reside in the Raleigh, North Carolina area.

A baseline measurement at the lowest possible stress voltage and current (lower V_{IN} for buck, higher V_{IN} for boost) should be taken before pushing the limits of power on the design once the setup is completed. Gate overshoot scales as a function of input voltage and output current, so if the design is marginal, it's best to discover and correct for this before stressing any limits. If the oscilloscope used for testing has reference cursors, it is helpful to place these at the upper and lower limits of the GaN V_G data sheet spec as a visual cue for tolerable ranges. Use the switch node waveform to trigger and overlay top and bottom gate waveforms to get the optimal picture of dead time. Ideally a differential or optical probe is used to measure top gate waveforms. If the measurement must be made with respect to ground, it is often helpful to use scope trace math functions (if available) to subtract switch node from top gate node inputs to have a virtual ground-based trace for analysis.

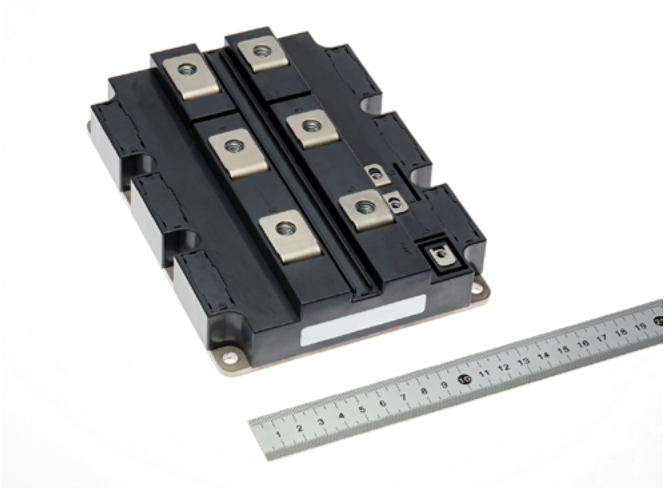
Conclusion

Proper techniques for laying out, probing, and collecting data outlined here should provide system designers with a good degree of confidence in the robustness of GaN-based designs implemented with the LTC7890 and LTC7891 step-down controllers. Once a prototype has been set up to accurately measure the switching waveforms on the bench, the designer can choose a configuration and then optimize the gate drive signals. This will be covered in "Smart GaN Buck Controller Designs - Part 2: Configuration and Optimization."

www.analog.com

High Voltage IGBT Modules

Mitsubishi Electric Corporation launched standard-isolation (6.0 kV_{rms}) and high-isolation (10.2 kV_{rms}) modules in its 4.5 kV/1,200 A XB Series of high-voltage IGBTs. These power semiconductors achieve high moisture resistance for more efficient and reliable inverters used in large industrial equipment, such as railcars, operating in diverse environments including outdoors. These modules (Dimensions 140 x 190 x 38 mm^3) use IGBT elements that incorporate Mitsubishi Electric's proprietary relaxed field of cathode (RFC) diode and carrier-stored trench-gate bipolar transistor (CSTBT1) structure. Specific structures for electric field relaxation and surface charge control enabled Mitsubishi Electric to reduce the chip's termination region size by about 30 % while also achieving about 20 times greater moisture resistance than existing products. In addition, the module reduces total switching loss by approximately 5 % compared to previous models, and reverse-recovery safe-operating area (RRSOA) tolerance is about 2.5 times greater than that of compared to previous models. By maintaining the same external dimensions as existing products for easy replacement, the module simplifies and shortens the process of designing new inverters.



www.mitsubishielectric.com

1200 V SiC Modules plies

SemiQ Inc has expanded its third-generation QSiC™ MOSFET product line by seven devices, including high-current S3 half-bridge (for example GCMX2P3B120S3B1-N), B2T1 six-pack (e. g. GCMX020A120B2T1P) and B3 full-bridge packages like the GCMX008B120B3H1P. The devices are engineered for current capabilities of up to 608 A and a junction-to-case thermal resistance of just 0.07 °C/W (in the 62 mm standard S3 half-bridge format). The six-pack modules integrate the three-phase power stage and have an R_{DSon} range of 19.5 to 82 mΩ. They are designed for motor drives and advanced AC/DC converters. The full-bridge modules deliver current capabilities of up to 120 A and an on-resistance down to 8.6 mΩ. This combination, coupled with a thermal resistance of 0.28 °C/W is intended e. g. for single-phase inverters and high-voltage DC/DC systems. The devices are breakdown voltage tested to over 1350 V.

www.semiq.com

High-efficiency synchronous-rectifier Controllers

STMicroelectronics' SRK1004 synchronous-rectifier controllers save space and increase efficiency in the secondary side of active-clamp, resonant, and quasi-resonant flyback (ACF, AHB, QR) converters for chargers, power adapters, and switched-mode power supplies. The minuscule 2mm x 2mm ICs supersede the SRK1001 and implement a new switch-off algorithm for increased efficiency and robustness.

With six variants available, the SRK1004 series lets designers choose logic-level or standard MOSFET gate drive, and 25ns or 150ns turn-off delay to compensate for drain inductance. Suitable for active clamp, resonant and quasi-resonant flyback topologies, the controllers also contain circuitry that creates a turn-on window to prevent unwanted switching. The output can sink up to 1.6A and source 0.6A to the gate, while the switching frequency of 500kHz permits a compact and low-cost design.

Leveraging ST's robust silicon-on-insulator (SOI) process, the SRK1004 can control the MOSFET in either low-side or high-side connection with up to 190V drain-source voltage. With a wide supply-voltage range, from 4V to 36V, the IC can be powered from the

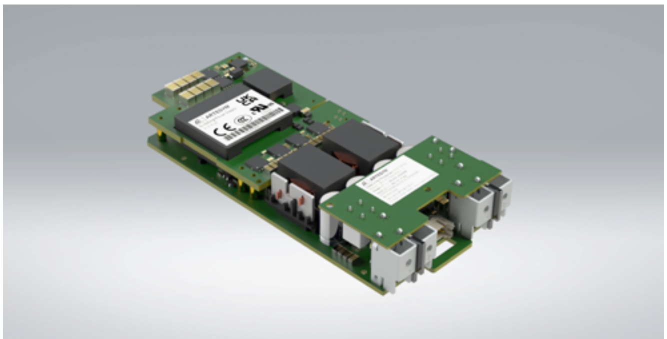
converter's output in a low-side configuration or from the transformer in a high-side configuration. This lets designers avoid providing a dedicated auxiliary power supply and so minimize the bill of materials. The SRK1004 contains a linear regulator that supplies the IC's internal circuitry and gate driver as well as providing power at an output pin for off-chip circuitry.

www.st.com

Dual-Output 400 W Module for Configurable Power Supplies

Advanced Energy Industries introduced a dual-output 24 V/24 V module for its NeoPower™ family of configurable power supplies, delivering up to 400 W (200 W per output) in a compact 2.5-inch form factor. This added module enables up to a total of 16 isolated outputs per power supply, streamlining system design for engineers in industrial, medical and test environments. Its power density is 18 W/in³. The digitally controlled module is certified according to IEC/EN/UL 62368-1 (industrial), IEC/EN 60601-1 (medical), and SEMI F47. Target applications include medical, industrial, semiconductor and test and measurement.

www.advancedenergy.com



Solder Paste for High Print Consistency and Easy Cleanability

Indium Corporation announced the global availability of SiPaste® C312HF, a halogen-free, cleanable solder paste formulated for fine-feature printing. Designed with Type 7 powder for aperture sizes down to 60µm, it enables fine-feature printing in advanced system-in-package applications.

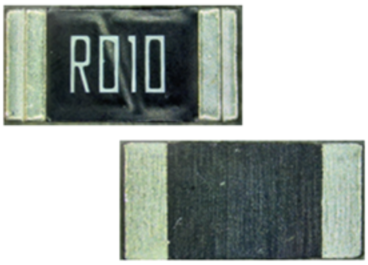
SiPaste C312HF boosts process yields that combine stencil print transfer efficiency and stencil life with consistent printing, response-to-pause, and reflow performance. SiPaste C312HF post-reflow flux residue can be cleaned with a standard cleaning process using semi-aqueous chemistries or a saponifier, or it can be used as a standard no-clean paste in processes where post-reflow cleaning is not required. Indium Corporation's SiPaste series is specifically designed for fine-feature printing with fine powders ranging from Type 5 to Type 8, including the SiPaste C312HF with Type 7 powder. The products help Avoid the Void®, reduce slumping, and demonstrate consistent superior printing performance.

www.indium.com

Current Sense Resistor

Stackpole's CSSU2512 current sense resistor shows a 5-watt power rating in a standard 2512 footprint. Its all-metal construction and thermally conductive design substantially achieves thermal performance on par with other 2512-size current sense chips rated at just 3 W. The devices are vailable in resistance values from 1 to 10 mΩ, with 1 % tolerance and a 50 ppm temperature coefficient of resistance (TCR). The resistor complies to AEC according to CSSU2512.

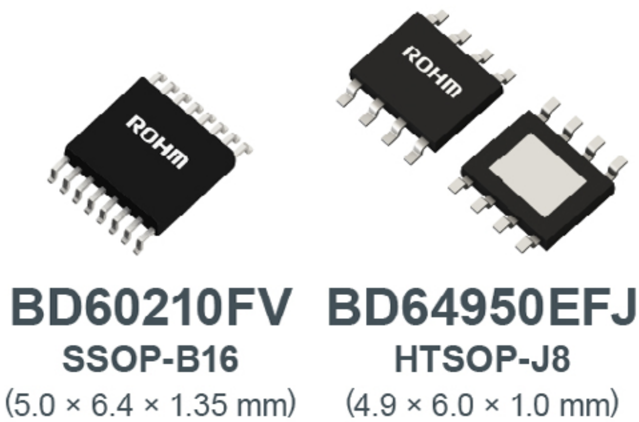
www.seielect.com



Brushed DC Motor Driver ICs

ROHM has developed two additional motor driver ICs for brushed DC motors, BD60210FV (20 V, 2 channels) and BD64950EFJ (40 V, 1 channel). They are intended for use in home and office appliances such as refrigerators, air conditioners, printers, and robotic vacuum cleaners.

The devices achieve a standby current of typically 0.0 µA (maximum: 1.0 µA). The BD60210FV can function as a dual H-bridge (2ch) motor driver with direct PWM control, capable of driving two DC brush motors, a bipolar stepper motor driver, or solenoid driver. Its H-bridge circuit configuration eliminates the need for a boost circuit, minimizing external components and contributing to space-saving and simplified design. It supports input voltage from 8 V to 18 V and 1 A/phase continuous current and 4 A/phase peak current. The BD64950EFJ features a single H-bridge (1ch) that supports both direct PWM control and constant current PWM control. Its low on-resistance design reduces heat generation. With a 40 V withstand voltage and 3.5 A continuous current (6 A peak), it is suitable for high-powered, high-voltage (24 V) DC brush motor applications.



www.rohm.com

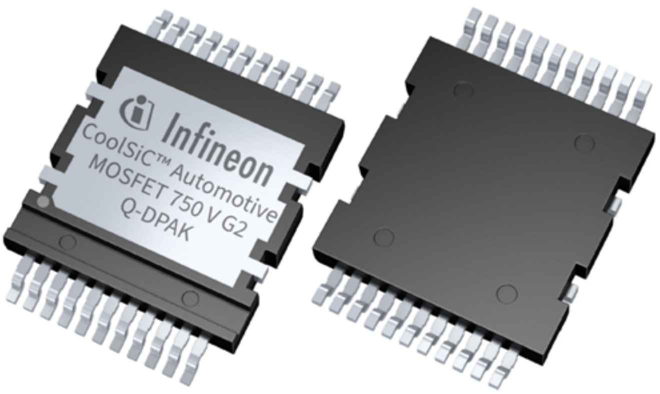
High-Voltage DC Contactors support Functional Safety

TDK Corporation introduced the HVC27*MC series of high-voltage DC contactors equipped with a mechanically linked, normally-closed auxiliary contact (mirror contact) compliant with IEC 60947-4-1. This feature provides precise contact position feedback for safety-critical applications in electric mobility and industrial energy systems. Measuring 86.5 x 95 x 44 mm^3 and "weighing" 530 g, these gas-filled contactors are suited for battery disconnect units (BDUs), energy storage systems (ESS), DC fast charging, and uninterruptible power supplies (UPS). Designed for DC voltages of 1000 V, the HVC27*MC series is available in 300 A, 400 A, and 500 A continuous current versions, with a single-shot capability of up to 900 A at 1000 V in less than 20 ms. The safety component is fully bidirectional with polarity-free main terminals. A hermetically sealed and gas-filled ceramic arc chamber takes care of a safe disconnection. The normally closed auxiliary contact reliably reports the main contact state, enabling the immediate detection of switching anomalies or failures. Offered in versions with 12 V or 24 V coil voltage and UL, CE, and UKCA certifications, the contactors are ready for global deployment. Typical applications are in commercial vehicles, industrial machinery, and high-voltage mobility systems.

www.tdk-electronics.tdk.com

750 V SiC MOSFET Family featuring new Packages

Infineon Technologies launches new packages for the CoolSiC™ MOSFET 750 V G2 technology, engineered to deliver high system efficiency and power density in automotive and industrial power conversion applications. This latest innovation is now available in a range of packages, including Q-DPAK and D2PAK, offering a portfolio with typical $R_{DS(on)}$ values up to 60 mΩ at 25°C.



The portfolio extension includes products for various applications, such as onboard chargers and HV-LV DCDC converters in the automotive sector, and server and telecom SMPS, along with EV charging infrastructure in the industrial applications. The low $R_{DS(on)}$ values of 4 mΩ enables applications that require exceptional static-switching performance, such as eFuse, high-voltage battery disconnect switches, solid-state circuit breakers, and solid-state relays. This performance enables designers to create more efficient, compact, and reliable systems that meet the most demanding requirements.

One of the key features of the CoolSiC MOSFET 750 V G2 technology is its innovative top-side cooled Q-DPAK package, which provides optimal thermal performance and reliability. This package is designed to handle high-power applications with ease, making it an attractive choice for designers seeking to push the boundaries of power density and efficiency. The technology also exhibits excellent $R_{DS(on)}$ x Q_{OSS} and best-in-class $R_{DS(on)}$ x Q_{fr}, contributing to reduced switching loss in both hard-switching and soft-switching topologies with superior efficiency in hard-switching user cases.

www.infineon.com

Plastic Transient Voltage Suppressors

Microchip Technology announces the release of its JANPTX family of non-hermetic plastic Transient Voltage Suppressor (TVS) devices that meet the MIL-PRF-19500 qualification, offering high-reliability protection for aerospace and defense applications. These TVS devices achieve MIL-PRF-19500 qualification in a plastic package, offering engineers a lightweight, cost-effective solution without sacrificing stringent military performance requirements.

The JANPTX product line is available in voltage ranges from 5V to 175V and includes five variants: JANPTX1N5555UJ, JANPTX1N5558UG, JANPTX1N5629AUJ, JANPTX1N5665AUG, JANPTX1N5907UG and JANPTX1N5907UJ.

With a high peak pulse power rating of 1.5 kW and clamping response times measured at less than 100 picoseconds in internal tests, the JANPTX family is designed to help ensure the safety and reliability of sensitive electronic components in demanding environments. Designed for surface mounting, these unidirectional TVS devices deliver protection against voltage transients such as lightning strikes, electrostatic discharge (ESD), and electrical surges.

The JANPTX TVS devices help safeguard airborne avionics, electrical systems and other mission-critical applications where low voltage and high reliability are essential. Their advanced design supports protection from switching transients, induced RF effects, Electromagnetic Pulse (EMP) and secondary lightning events, designed to meet IEC61000-4-2, IEC61000-4-4, and IEC61000-4-5 standards.

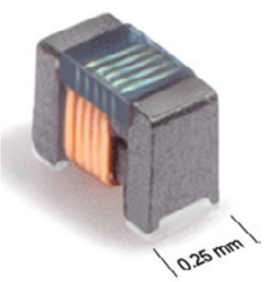
www.microchip.com

PMIC capable of harvesting full-range of hybrid indoor-outdoor PV Cells

e-peas made the public debut of its AEM15820 power management IC (PMIC), the a single-chip PMIC capable of spanning the full dynamic range of hybrid indoor-outdoor PV cells. These hybrid PV cells have a wide power output that can vary from microwatts under indoor lighting to several watts when in direct sunlight. To manage this range, multi-PMIC solutions have previously been required, adding cost and complexity to the overall system designs.

They are being implemented in a wide range of consumer applications, including sports or hiking computers and self-charging headphones, and will enable many more, such as PV-charged earbud cases and e-readers. Additional markets include remote security cameras, smart glasses, power banks, and smart-backpack power modules. It is optimized for use with both batteries and lithium-ion capacitors (LiC) and features an ultra-low-power cold start of 5 µW at 275 mV.

www.e-peas.com



Small Ferrite-Core wirewound Chip Inductors

The 016008F series is claimed to be the world's smallest wirewound ferrite chip inductor, designed for high-frequency applications where board space is constrained. With dimensions of 0.5 mm x 0.25 mm x 0.38 mm, it offers a DCR of 0.18 Ohms. Typical applications are compact devices such as smartphones, IoT modules, and wearables.

www.coilcraft.com

FOC-based BLDC Motor Control with Power Regulation up to 15A

BLDC FOC 2 Click is a motor control Click board™ from MIKROE. The compact Click add-on boards enable developers to rapidly provide proof-of-concept, then prototype and code new embedded projects. BLDC FOC 2 Click provides provides robust and reliable control of three-phase brushless DC (BLDC) motors using advanced Field-Oriented Control (FOC) techniques, ensuring smooth operation, high efficiency and low acoustic noise.

Comments Nebojsa Matic, CEO of MIKROE: "This new Click board is ideal for automotive and industrial applications such as battery cooling fans, radiator fans, and fuel or oil pump control systems. It is part of our 140+ strong family of motor control Click boards and over 850 projects - with working code - featuring the BLDC FOC 2 Click can be found on MIKROE's embedded projects platform, EmbeddedWiki."

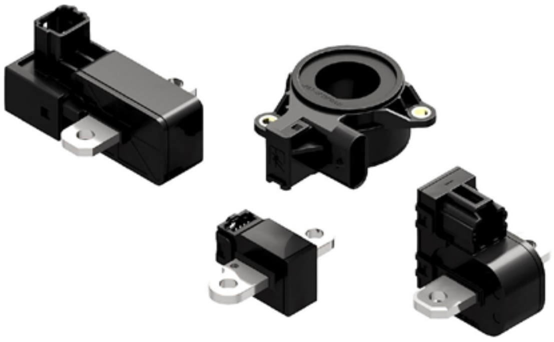
BLDC FOC 2 Click is based on the A89307, an automotive FOC BLDC motor controller from Allegro Microsystems, designed to deliver up to 15A of output current across a wide voltage range from 4.4V to 30V. It supports multiple operating modes, including constant speed, torque, power and open-loop control, while offering flexible

configuration via EEPROM and I2C interface for parameter setting, ON/OFF control and speed feedback. It also integrates Allegro's proprietary Soft-On Soft-Off (SOSO) feature for quiet transitions, comprehensive protection mechanisms, and both analog and digital control mode.

www.mikroe.com

Open-loop hall-effect Current Sensors for electric and hybrid Vehicles

Littelfuse announced the release of six new automotive current sensors designed to enhance electric and hybrid vehicle performance, efficiency, and functional safety. The Littelfuse automotive qualified sensors provide precise, isolated current measurement across battery-management, motor-control, and pyro-fuse safety systems. Utilizing open-loop hall-effect technology, the sensors



deliver reliable performance in compact, bus-bar-mounted form factors. Output configurations include analog-voltage and digital (CAN/LIN) communication, giving system designers flexibility in integrating with existing EV architectures.

As EV and hybrid systems evolve, engineers face growing demands for high accuracy, fast response, and compliance with functional-safety standards. This current-sensor family helps OEMs and Tier 1 suppliers meet those challenges by offering scalable, ASIL-capable solutions that simplify design while improving efficiency, safety, and overall system reliability.

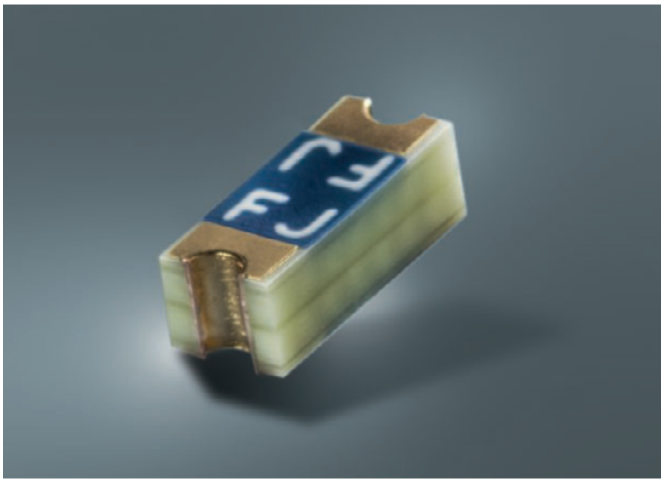
Across the automotive qualified product family, nominal current ranges extend up to ±1500 A, with high total-error performance and minimal thermal drift. Models featuring CAN 2.0B communication include AUTOSAR E2E Profile 1A diagnostics and ASIL-C-capable current measurement, enabling integration into safety-critical systems such as battery control or disconnect units.

www.littelfuse.com

Surface-Mount Fuse

With the Surface-Mount Fuse USE 2410 SCHURTER introduces a quick-acting F fuse which is completely without internal solder joints. AEC-Q200 tested, sealed against potting compounds and designed for extreme temperatures, the USE 2410 provides is intended for protection in applications ranging from industrial and automotive to medical technology. It is designed for 125-250 V_{AC} and 86-125 V_{DC}. In the temperature range from -55 °C to 125 °C the breaking capacity is up to 200 A, while the rated currents are specified from 0.6 to 10 A. Manufactured from UL 94V-0 materials – fiber-reinforced plastic and gold-plated copper terminals – the fuse is certified to UL, VDE, RoHS and REACH. Typical applications include battery-operated systems, LED drivers, ballasts, medical and industrial equipment, power supplies, and white goods. In automotive (IATF 16949) or aerospace, it protects against overload and short circuit.

www.schurter.com



NPN and PNP Bipolar Transistors for Compact Automotive Designs

Diodes announces an expansion of its automotive-compliant bipolar transistor portfolio with the introduction of the DXTN/P 78Q & 80Q series. These low VCE(sat) NPN and PNP transistors deliver conduction efficiency and thermal performance, optimized for demanding automotive power switching and control.

The twelve devices support a broad voltage range, making them suitable for 12V, 24V, and 48V automotive systems. They are ideal for gate driving MOSFETs and IGBTs, power line and load switching, low-dropout (LDO) voltage regulation, DC-DC conversion, and driving motors, solenoids, relays, and actuators. Rated for continuous operation up to +175°C, and offering high ESD robustness (HBM 4kV, CDM 1kV), they provide reliable operation in harsh automotive environments.

Housed in the compact PowerDI®3333-8 package (just 3.3mm x 3.3mm), these devices cut PCB footprint by up to 75% versus traditional SOT223, freeing space for additional functionality. A large underside heatsink delivers ultra-low thermal resistance (RθJL) of 4.2°C/W. The side-wall plateable (SWP) feature improves automated optical inspection (AOI) visibility and strengthens solder joints. This enhances quality assurance, reduces manual inspection, and supports efficient, reliable manufacturing.

Both series span BVCEO ratings from 30V to 100V and deliver robust current handling. The DXTN/P 80Q series provides extra headroom for demanding designs, with continuous ratings up to 10A and peak pulse capability of 20A. Ultra-low saturation voltage (just 17mV at 1A) and an on-state resistance as low as 12mΩ minimize conduction losses, enabling cooler operation and higher efficiency. This helps designers cut conduction losses by up to 50% versus previous generations, reducing heat and easing thermal management.

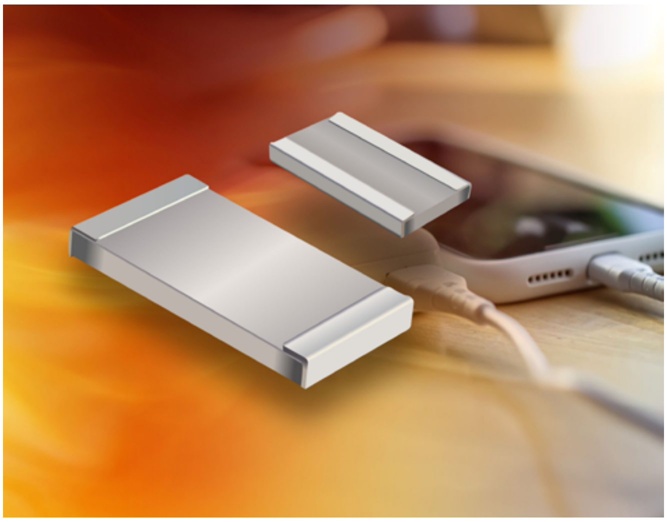
www.diodes.com

Thermal Jumper Chip Series

Bourns introduced its BTJ Series Thermal Jumper Chips designed to provide effective thermal dissipation in a compact form factor. These devices provide high thermal conductivity while also having insulating properties to help protect and prolong system component lifespans. Because the thermal jumper chips are able to quickly dissipate heat and do not conduct electricity, they have no impact on system operation.

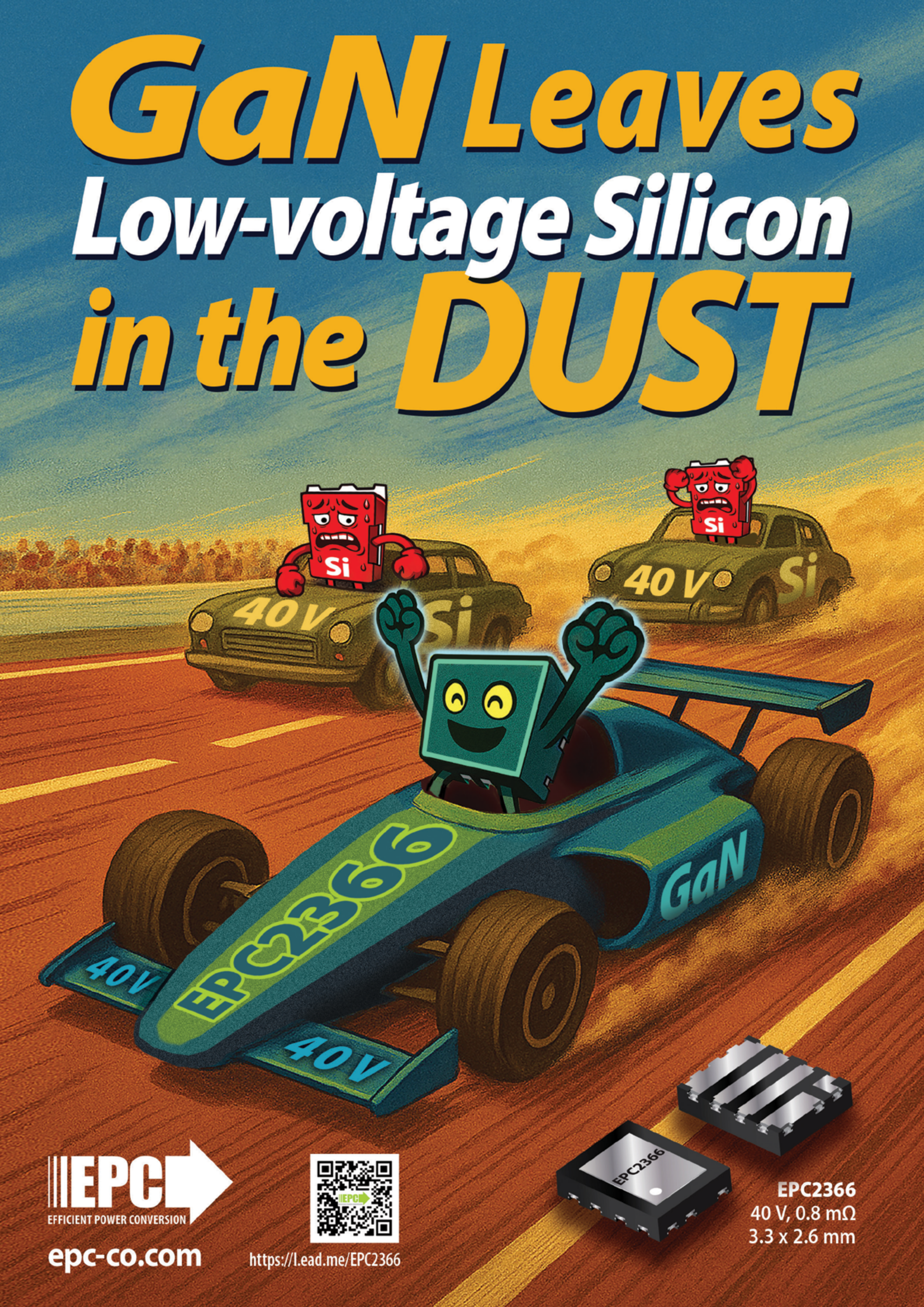
Available in SMD packaging, Bourns® Thermal Jumper Chips provide an excellent thermal dissipation solution for a variety of mobile devices and electronic equipment that include power supplies, converters and RF and GaN amplifiers. Furthermore, the advanced design takes advantage of the chips' insulating properties so the space between the heating element and the heat detection element can be filled to enable highly accurate heat detection. These features also help reduce the temperature rise of key components contributing to improved reliability at the system level.

The Bourns® BTJ Series Thermal Jumper Chips are available now and are RoHS compliant and halogen free.



ww.bourns.com

Advertising Index



GaN Leaves
Low-voltage Silicon
in the DUST
Si
40 V
Si
Si
40 V
Si
EPC2366
GaN
40V
40V
EPC2366
EPC
EFFICIENT POWER CONVERSION
epc-co.com
https://l.ead.me/EPC2366
EPC2366
40 V, 0.8 mΩ
3.3 x 2.6 mm